

AC-F-3065-3
1 JULY 1967

FINAL REPORT
VOLUME III

Prepared for
INSTRUMENTATIONS AND COMMUNICATIONS DIVISION
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AROD TEST MODEL HARDWARE
FINAL REPORT
CONTRACT NO. NAS8-11835

AROD SYSTEM
FINAL REPORT
AC-F-3065-3

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SECTION VI

6. TRANSPONDER STATION

The function of the Transponder Station is to receive, translate, and retransmit signals containing a ranging code from an AROD Airborne Vehicle. The Transponder is capable of automatic acquisition and tracking thus allowing the use of unmanned ground stations. To achieve these objectives, two receivers are utilized; a VHF receiver for rapid acquisition and station control and an S-Band receiver for tracking.

Constraints not usually found in ground equipment were put on the transponder with respect to size, weight, and power requirements. Although the transponder is rack mounted for convenience during feasibility studies, the two receivers and power system, being self-contained in separate drawers, can be individually enclosed. This results in units which are easily transportable and versatile in their power source requirements.

Common designs between Vehicle and Transponder equipments were utilized wherever possible. Vehicle cordwood modules are used wherever receiver designs coincided.

To maximize reliability, all components were chosen to operate at 25% of their voltage, current, or power ratings unless constrained by other factors. Also, integrated circuits were employed whenever practical.

The Transponder Station consists of two receivers and a Transmitter. The Station Control Receiver receives a 138 MHz PSK/PM/PM signal which contains all instructions for the transponder. The Station Tracking Receiver receives a 2214 MHz PN/bi-phase modulated signal and the transmitter retransmits the same code at 1800 MHz. A functional block diagram of the Transponder Station is shown in Figure 6-1. Brief descriptions of Transponder Station functions follow.

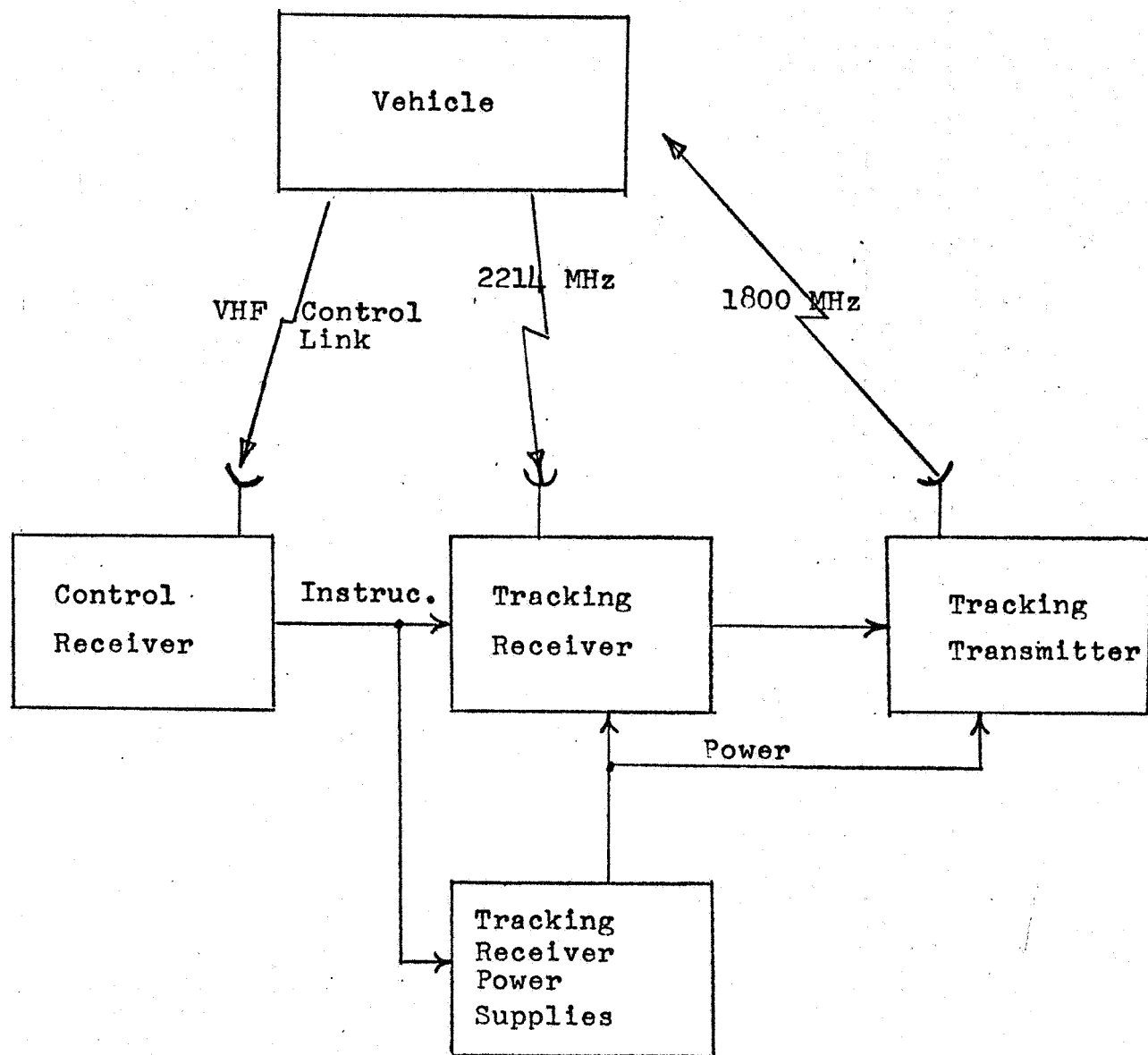


Figure 6-1. AROD Transponder

6.1 PHYSICAL DESCRIPTION

External physical details of the Transponder Station Rack are shown in Figures 6-2 and 6-3. The rack is a 41-inch standard 19-inch cabinet containing four assemblies. The assemblies are listed in Table 6-1. The TWTA assembly is a 15-inch by 30-inch plate containing the TWTA, a fan, output signal filters, and a small control panel.

TABLE 6-1. List of Assemblies

| Assembly | Name |
|----------|---------------------------|
| 1A1 | Station Control Receiver |
| 1A2 | Station Tracking Receiver |
| 1A3 | Power Amplifier |
| 1A4 | AC/DC Converter |
| --- | TWTA Assembly |

Rack power and R-F signal connections are made at the connector panel at the rear of the rack, shown in Figure 6-3.

The top assembly is the Station Control Receiver (1A1). The next lower assembly is the Station Tracking Receiver (1A2). Third assembly is the Power Amplifier (1A3) and the bottom assembly is the AC/DC converter (1A4).

Station monitor jacks for interconnection to the Transponder Check-Out Equipment are located in the front lower right-hand corner of each assembly. Memory loading interconnection jacks are located in the front lower left-hand corner of the Station Control Receiver (1A1).

Assemblies 1A1, 1A2, and 1A3 are slide mounted drawers with dust tight covers. The AC/DC converter assembly 1A4 is mounted directly to the cabinet. A convenience 110 VAC raceway with five jacks is provided inside the rack for test equipment power.

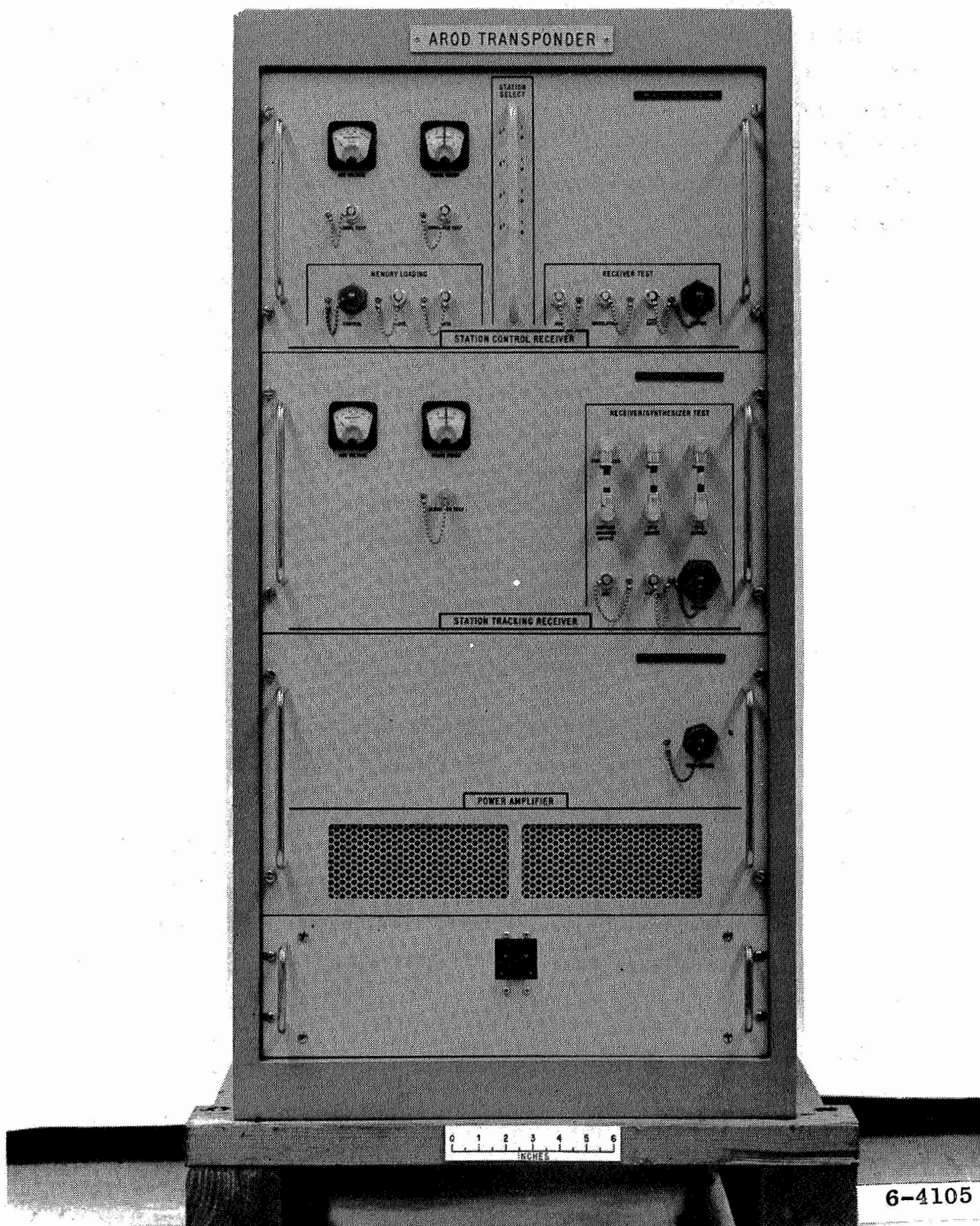


Figure 6-2. Transponder Rack, Front View

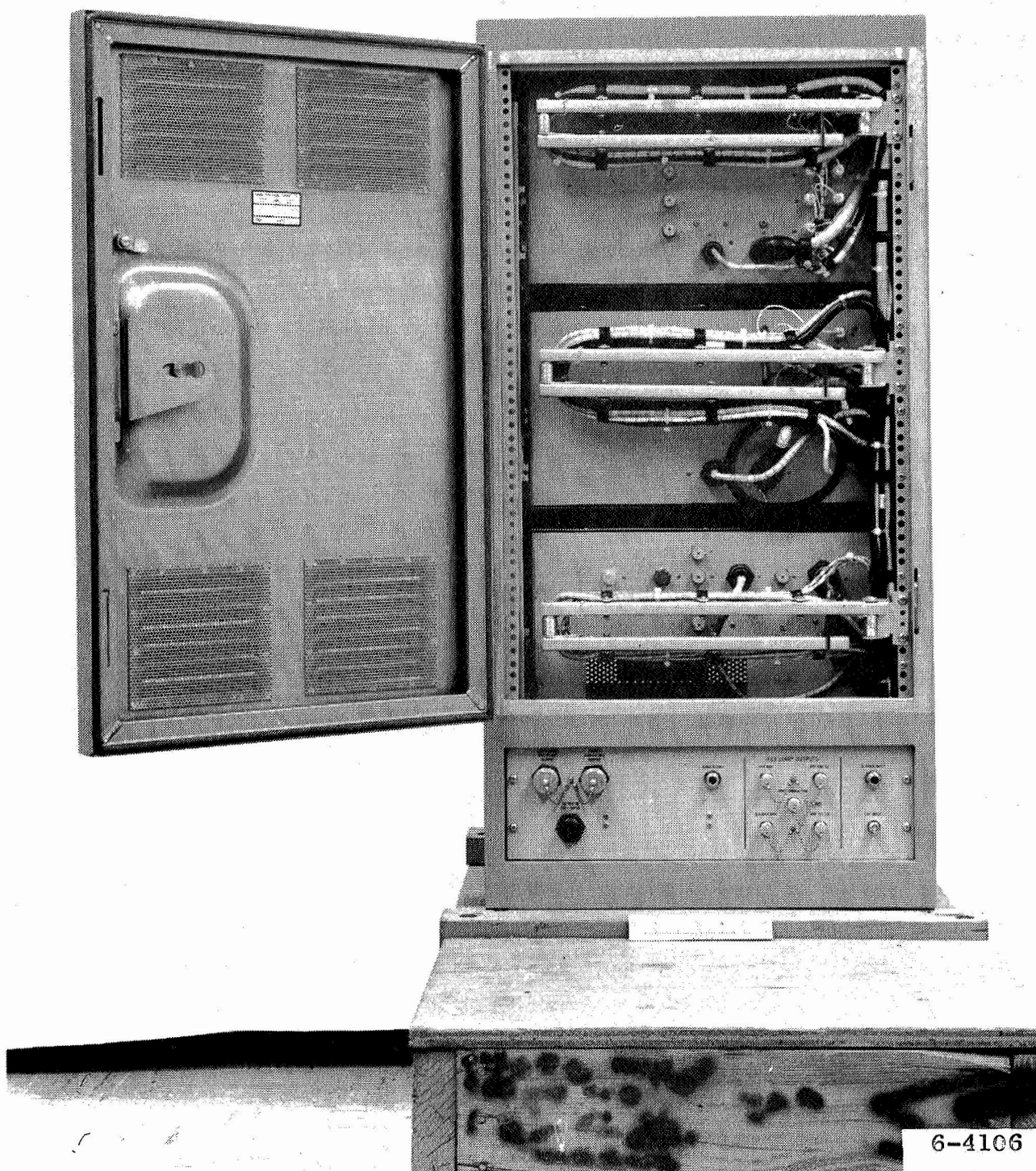


Figure 6-3. Transponder Rack, Rear View

6.1.1 Station Control Receiver (1A1)

The Station Control Receiver is a panel and chassis assembly containing sixteen modular assemblies including three power supplies, three 6 x 6 digital cards, and ten R-F modules. See Figure 6-4. Location of the modules is shown in Figure 6-5. Module identifications are given in Table 6-2.

The front panel contains two meters, (receiver AGC and dynamic phase error), two R-F test signal jacks, (3.2 MHz and 17 MHz) and four toggle switches for setting the station identification code. Test outputs and memory loading jacks are also provided. Receiver input and output signals and assembly power are connected at the rear panel through 11 R-F jacks and two MS connectors. Four fuses are also mounted on the rear panel.

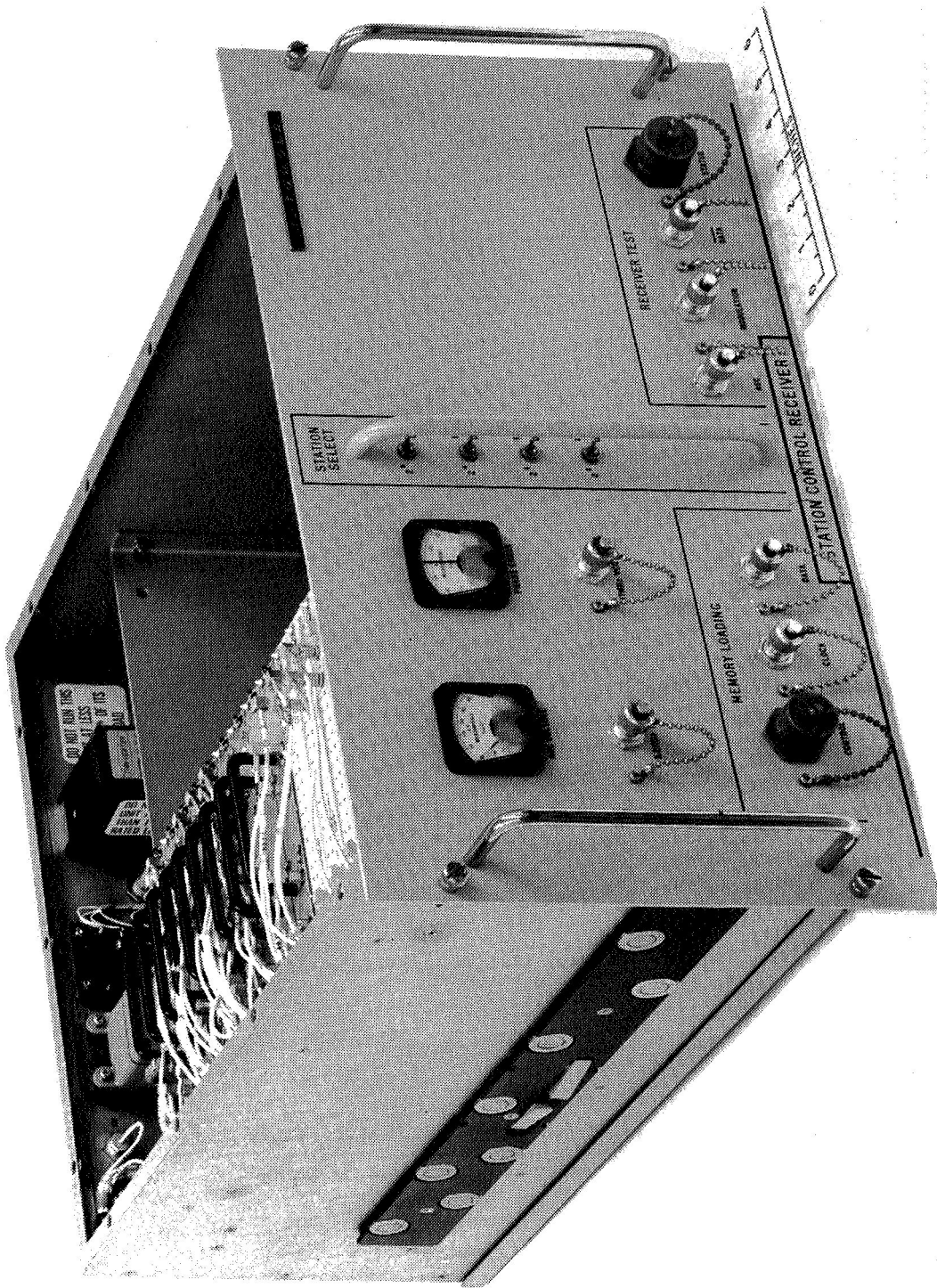
One spare R-F module space and one spare digital 6 x 6 card space is provided. Space is also available for the addition of up to 13 modules and/or digital cards for future expansion of assembly functions.

6.1.2 Station Tracking Receiver

The Station Tracking Receiver is a panel and chassis assembly containing 22 modular assemblies including, three 6 x 6 digital cards and 19 R-F modules. See Figure 6-6. Location of the modules is shown in Figure 6-7 and module identifications are given in Table 6-3

The front panel contains: two meters, (receiver AGC and dynamic phase error); two R-F test signal jacks, (12.8 MHz VCO and receiver AGC); and assorted test jacks. Receiver input and output signals and assembly power are connected at the rear panel through seven R-F jacks and two MS connectors. A TEST/OPERATE switch is also mounted on the rear panel

Two spare R-F module spaces are provided in the receiver.



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Figure 6-4. Station Control Receiver (Top Dust Cover Removed)

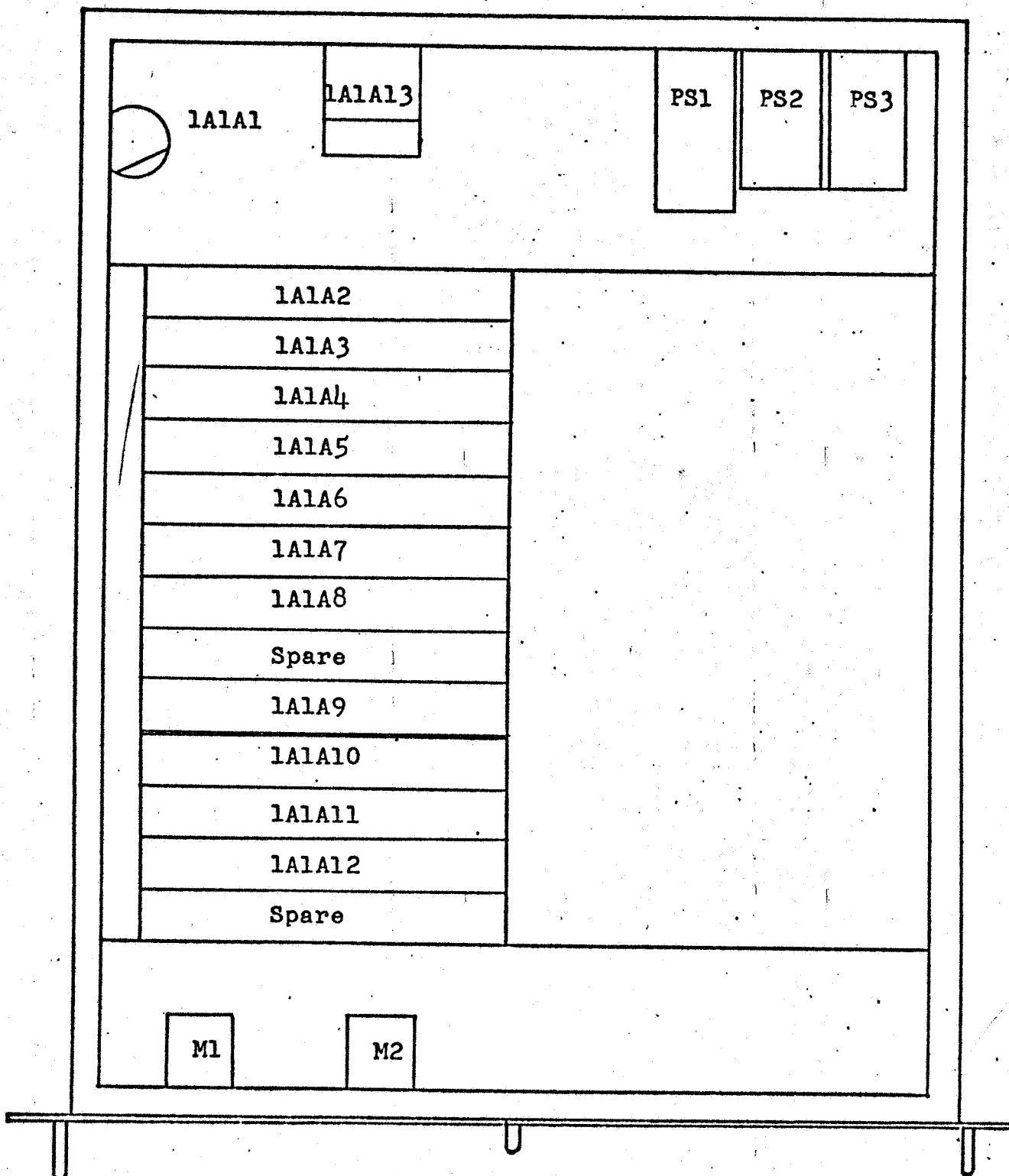
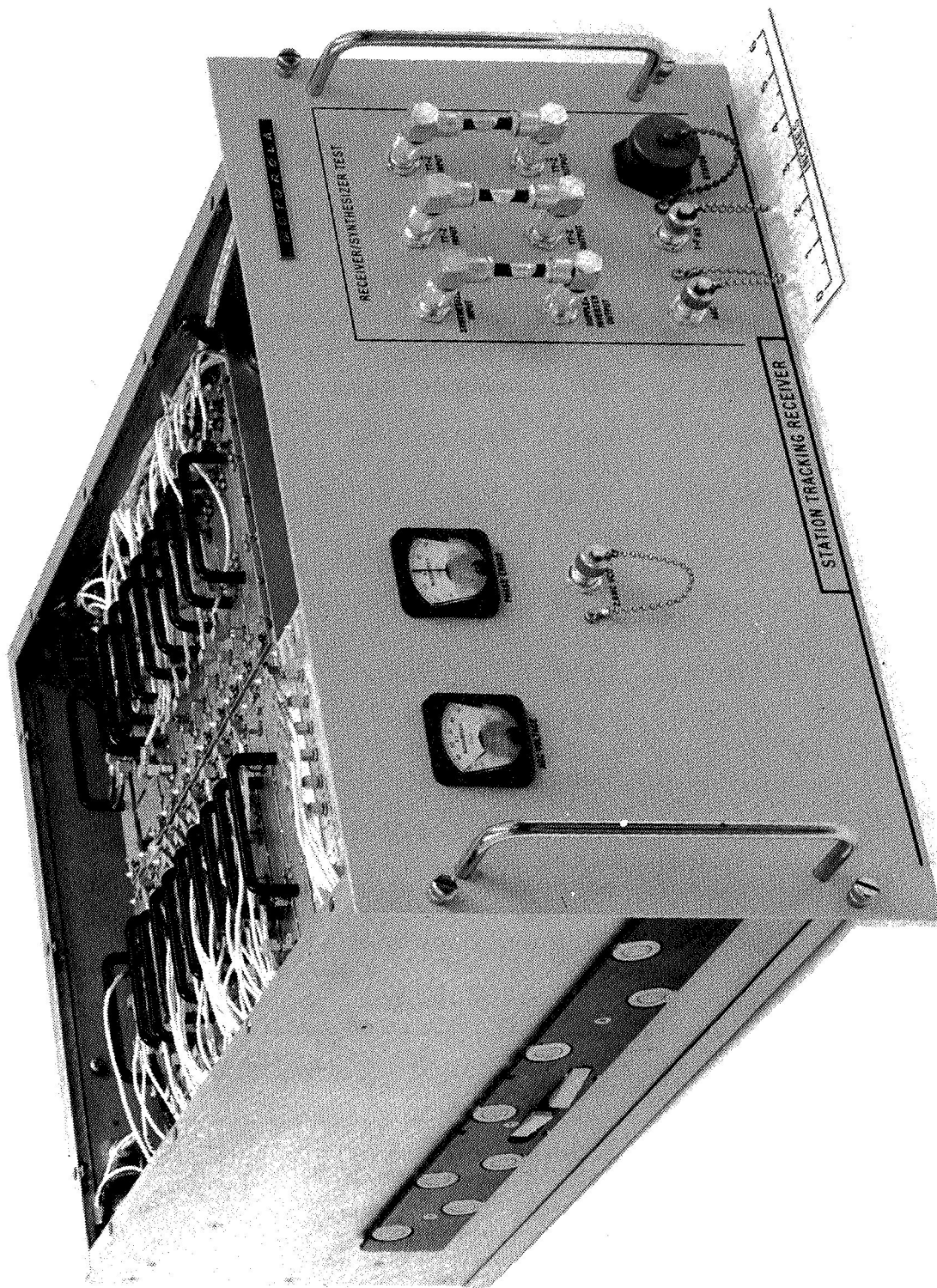


Figure 6-5. Station Control Receiver Module Location



6-4108

Figure 6-6. Station Tracking Receiver (Top Dust Cover Removed)

TABLE 6-2. Station Control Receiver Module Locations

| Module | Title |
|--------|-----------------------------|
| 1A1A1 | Filter, Bandpass, VHF |
| 1A1A2 | Converter, Freq - VHF |
| 1A1A3 | Ampl, I-F - AGC |
| 1A1A4 | Gen, LO - REF |
| 1A1A5 | Osc, Voltage Cont. - 17 MHz |
| 1A1A6 | Det., Radio Freq |
| 1A1A7 | Synth, Freq |
| 1A1A8 | Osc, Freq. Preset |
| 1A1A9 | Freq Divider, Freq Preset |
| 1A1A10 | Data Demod No. 1 |
| 1A1A11 | Data Demod No. 2 |
| 1A1A12 | Logic, Station Control |
| 1A1A13 | Osc, Ref - 3.2 MHz |
| PS1 | +3.5 Volt Supply |
| PS2 | -9 Volt Supply |
| PS3 | +9 Volt Supply |

TABLE 6-3. Station Tracking Receiver Module Location

| Reference Designation | Module Name |
|-----------------------|---|
| 1A2A1 | Converter, Frequency S-Band |
| 1A2A2 | Frequency Multiplier X14 |
| 1A2A3 | Frequency Multiplier X5/16 |
| 1A2A4 | Oscillator, Voltage Controlled 12.8 MHz |
| 1A2A5 | Mixer, Intermediate Frequency 8 MHz |
| 1A2A6 | Amplifier, Intermediate Frequency 8 MHz |
| 1A2A7 | Detector, Radio Frequency 8 MHz |
| 1A2A8 | Detector, Radio Frequency- Ranging Loop |
| 1A2A9 | Detector, Radio Frequency- Frequency Preset |
| 1A2A10 | Mixer, Doppler |
| 1A2A11 | Detector, Radio Frequency 38.4 MHz |
| 1A2A12 | Oscillator, Voltage Controlled- Doppler |
| 1A2A13 | Doppler Sign Detector |
| 1A2A14 | Mixer, Synthesizer Loop |
| 1A2A15 | Frequency Divider, Synthesizer Loop |
| 1A2A16 | Oscillator, Voltage Controlled- Synthesizer Loop |
| 1A2A17 | Frequency Multiplier/Modulator X2 |
| 1A2A18 | Frequency Multiplier/Modulator X8 and X4 |
| 1A2A19 | Code Control No. 1 |
| 1A2A20 | Code Control No. 2 |
| 1A2A21 | Bias Converter - Filter |
| 1A2A22 | Acquisition Unit |

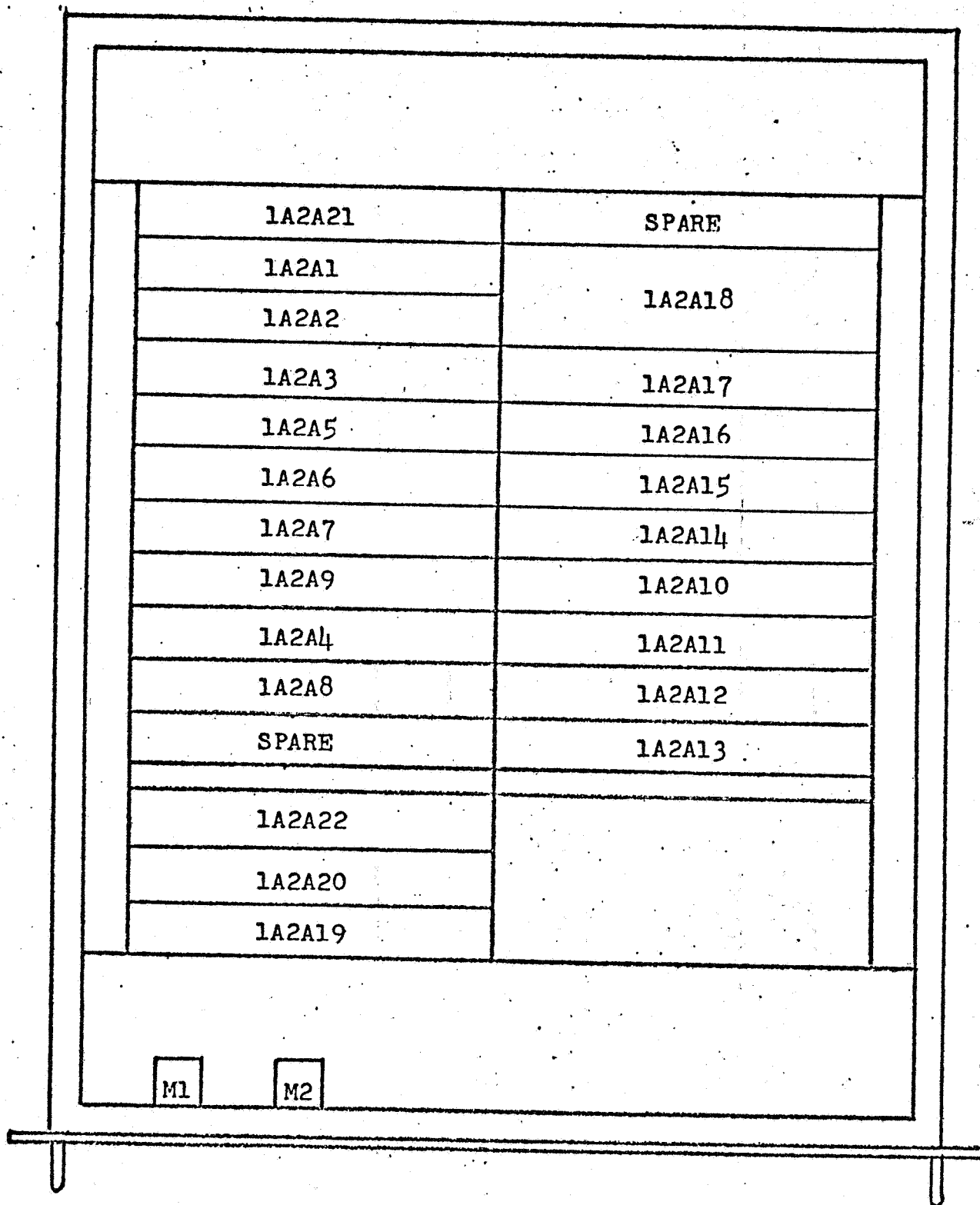


Figure 6-7. Station Tracking Receiver Module Location

6.1.3 Power Amplifier (1A3)

The power amplifier is a panel and chassis assembly with thermal floorplate. Figure 6-8 is a top view of the drawer and Figure 6-9 shows the layout. Four DC/DC converters, one filter, three terminal boards, a relay assembly, and two thermal switches are mounted on the top side of the thermal plate. A blower is mounted on the lower side. Driver circuitry is located on the relay assembly.

Two multipin jacks are mounted on the rear panel to carry power in and out of the drawer. Five fuses and two R-F jacks are also mounted on the rear of the drawer. The front panel contains one multipin jack.

6.2 STATION CONTROL RECEIVER

This subsection is devoted to the discussion of the station control drawer. Five essential functions are covered as shown in Figure 6-10.

1. Control Receiver
2. Preset Synthesizer
3. Reference Synthesizer
4. Control Data Demodulator
5. Control Logic

6.2.1 Control Receiver

The basic requirements for the Control Receiver are:

1. Acquire and phase lock to a VHF 138 MHz phase modulated signal having ± 6 kHz of Doppler offset, with levels from -60 dBm to -130 dBm.
2. Acquire and lock to the above signal in minimum time.
3. Be tunable from 135 to 150 MHz in 25 kHz increments.

Carrier Loop

A functional block diagram of the VHF receiver carrier loop is shown in Figure 6-11.

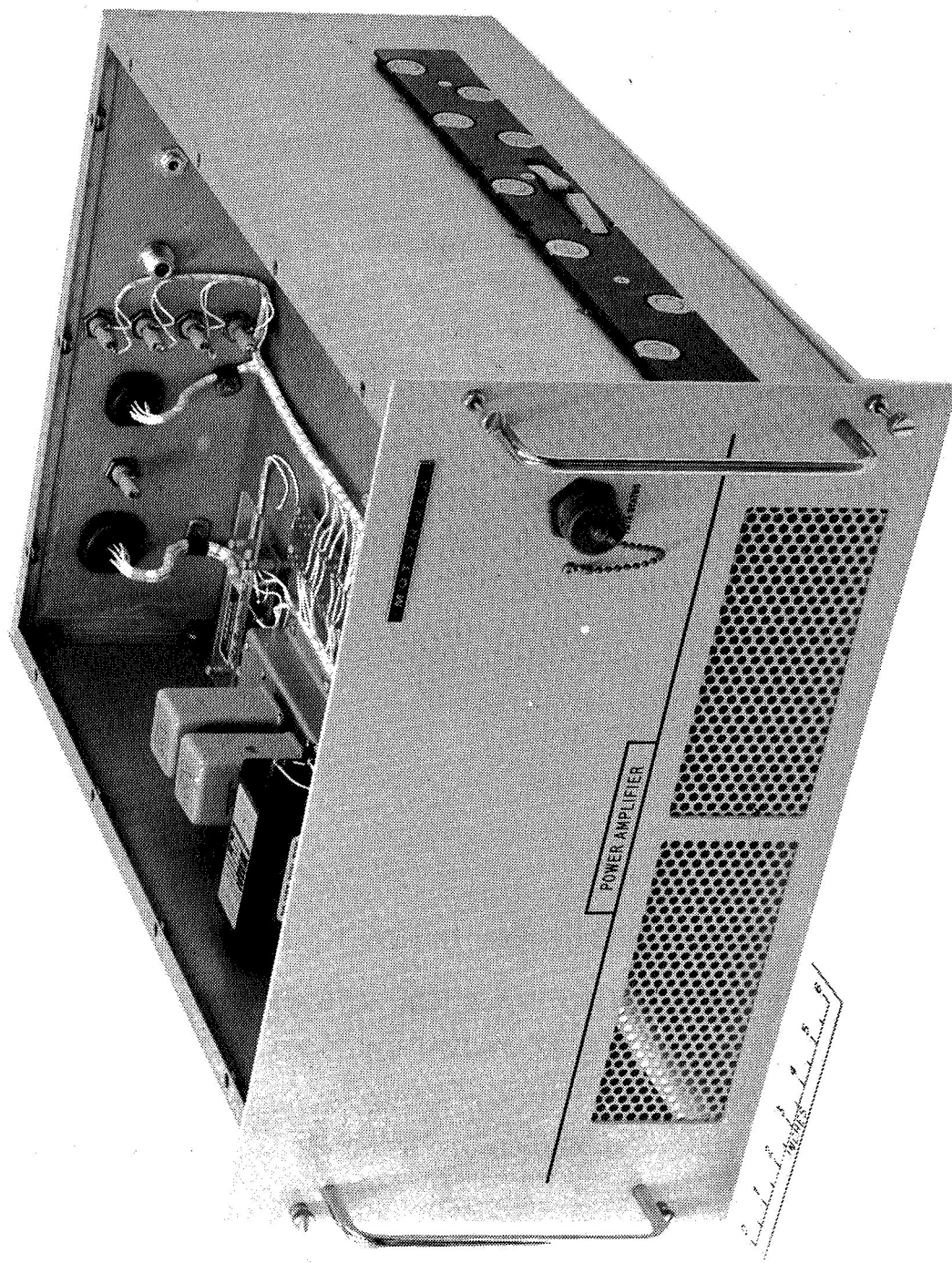


Figure 6-8. Power Amplifier (Top Dust Cover Removed)

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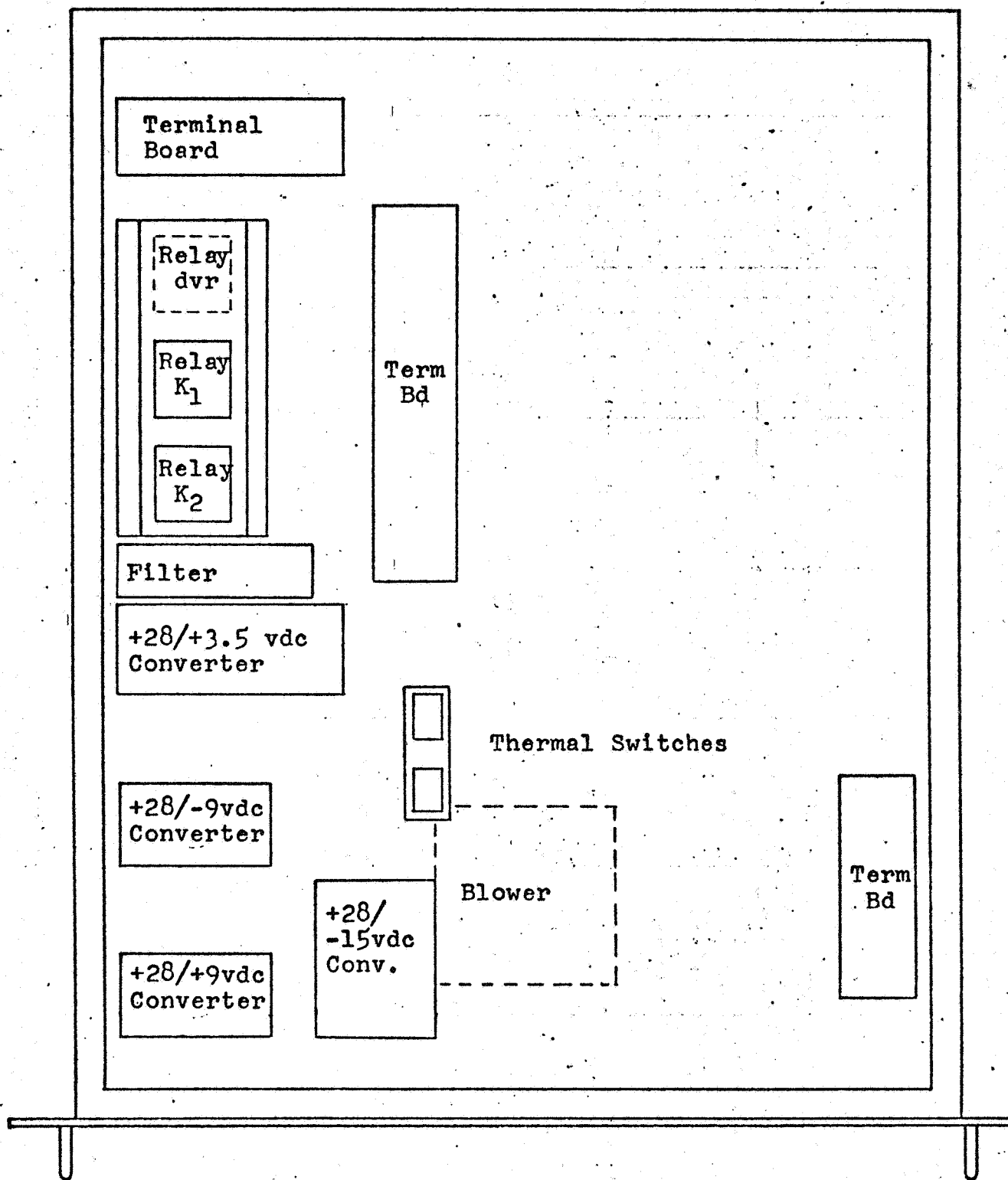


Figure 6-9 . Station Power Amplifier (1A3) Physical Layout

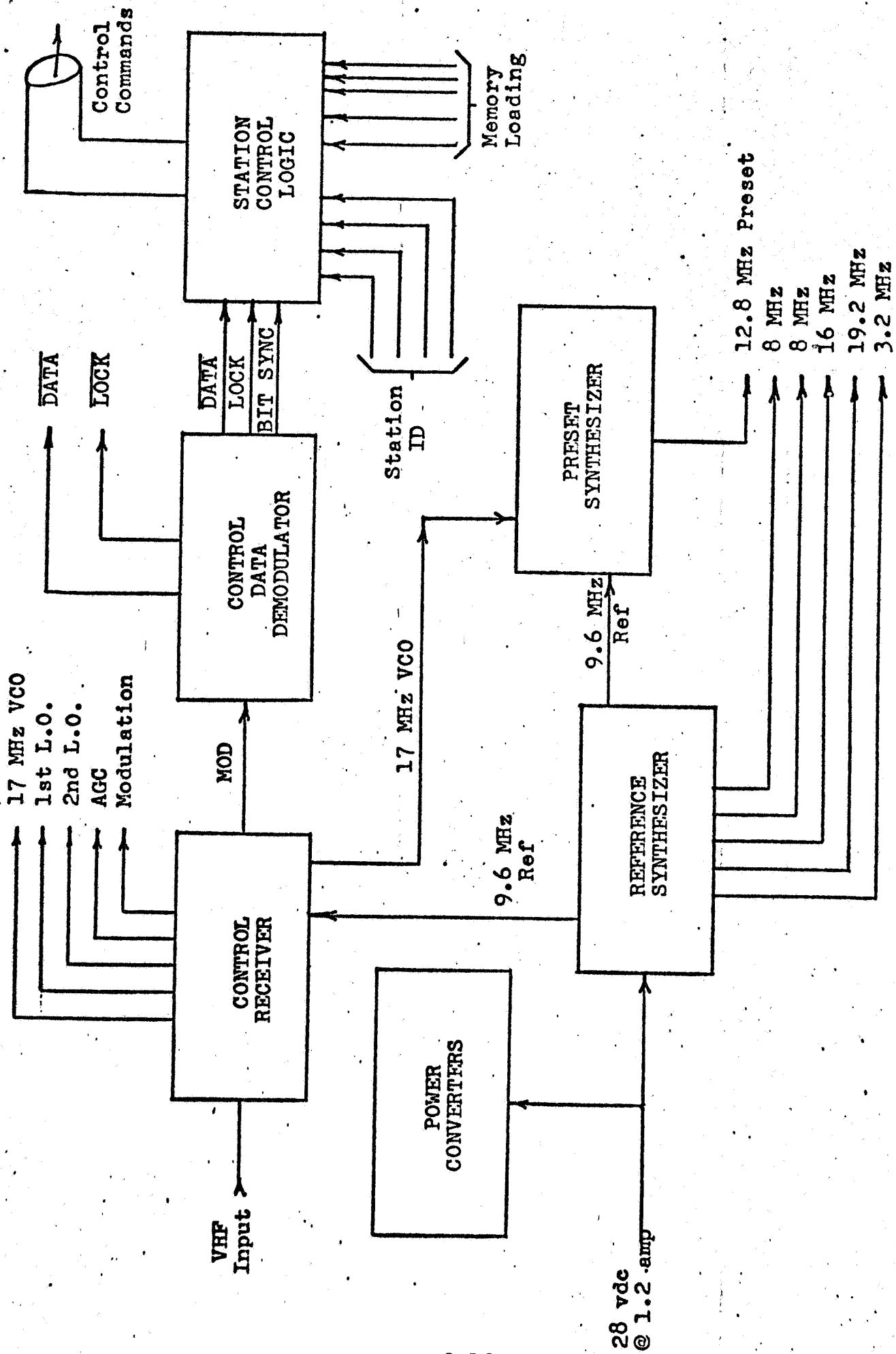


Figure 6-10. Station Control Receiver

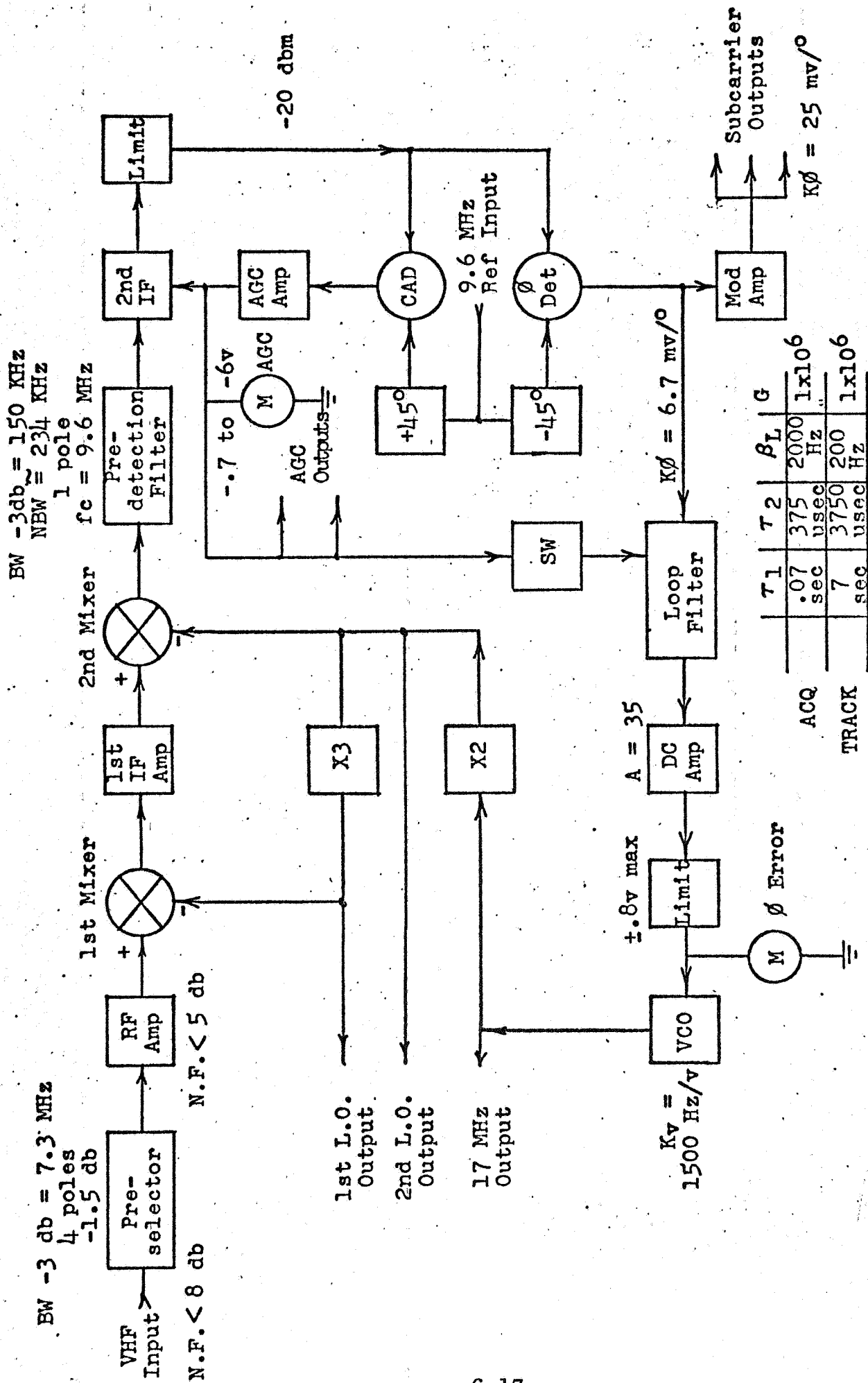


Figure 6-11. Station Control Receiver Functional Block Diagram

The receiver is a narrow band, carrier tracking system approximating a Type-one, second order servo loop. A wide loop bandwidth is provided for rapid carrier acquisition which switches to a narrow band loop after acquisition to give the desired threshold characteristics.

The loop is linear, i.e., without a limiter, so that the loop noise bandwidth is essentially constant over all signal level conditions. The receiver also contains a coherent AGC system. Signal flow is as follows:

The input signal is passed through a four-section preselector with a 7 MHz bandwidth to reduce interference signals and then amplified before conversion to the first I-F frequency. The amplifier reduces receiver noise figure and attenuates local oscillator signal flows back to the signal input jack. The input signal is then converted to a first I-F frequency of approximately 42 MHz in a double balanced mixer. The mixer is wideband and does not contain tuning or balance adjustments.

The signal is amplified at the first I-F frequency and converted to the second I-F frequency in a second balanced mixer. The resultant 9.6 MHz signal is passed through a 150 kHz predetection filter and then fed to the second I-F amplifier where gain control is accomplished. A limiter is used at the second I-F amplifier output to prevent noise from unbalancing the loop phase detector when the loop is unlocked. However, the limiter threshold is set above the signal plus RMS noise power level so that signal suppression does not occur at threshold signal levels. The 9.6 MHz signal is phase compared to a local 9.6 MHz reference signal generated from the Station Master Oscillator and the resulting D-C error voltage is filtered and amplified in the loop filter.

The loop filter output is then used to control the loop voltage controlled oscillator. The VCO frequency is multiplied by X2 and X3 to generate the first and second local oscillator signals, thus closing the loop. A second limiter output is fed to a coherent amplitude detector and the CAD output is filtered and

amplified to form the AGC voltage used to gain control the second I-F signal.

The predetection filter is sufficiently wide to pass modulation signals on the carrier so that the loop detector provides the demodulated 18.75 kHz subcarrier. The subcarrier, containing coded control signals is amplified and fed to the data demodulator circuitry.

Loop bandwidth switching is accomplished by changing loop filter time constants. This is done by increasing the filter resistance when the receiver is locked, by using the AGC voltage to control an FET gate.

The receiver loop is optimized (i.e., the damping factor adjusted to be 0.707) for an input carrier signal level of -130 dbm. The loop gain distribution is as follows:

| | |
|-----------------------|--------------------------|
| Loop gain | 10^6 secs^{-1} |
| Phase detector gain | 6.7 millivolts/degree |
| VCO gain | 1500 Hz/volt |
| Loop filter D-C gain | 35 volts/volt |
| Frequency multipliers | 8 |

With the given loop parameters, it would normally be possible to acquire an 18.75 kHz sideband instead of the carrier I-F Doppler shift were maximum. Sideband lock is precluded by limiting the control voltage output of the phase loop D-C Amplifier.

Local Oscillator Selection

It is required that the VHF receiver be tunable in 25 kHz steps to receiver signals from 135 to 150 MHz.

The frequency of the local oscillator is related to the input frequency as follows.

$$f_v = \frac{f_{in} - f_r}{N}$$

f_r = Detector reference = 9.6 MHz

N = LO multiplier = 8

$$\therefore f_r = \frac{f_{in} - 9.6}{8}$$

Since f_{in} varies in 25 kHz steps f_v will vary in $25/8 = 3.125$ kHz steps.

For a 138 MHz input

$$f_v = \frac{138 - 9.6}{8} = 16.05 \text{ MHz}$$

Preset Synthesizer

The function of the Preset Synthesizer is to develop a 12.8 MHz signal containing a Doppler shift which is directly proportional to that of the input signal. This 12.8 MHz signal is then used as a reference to preset the Tracking Receiver local oscillator thus eliminating frequency search at S-band.

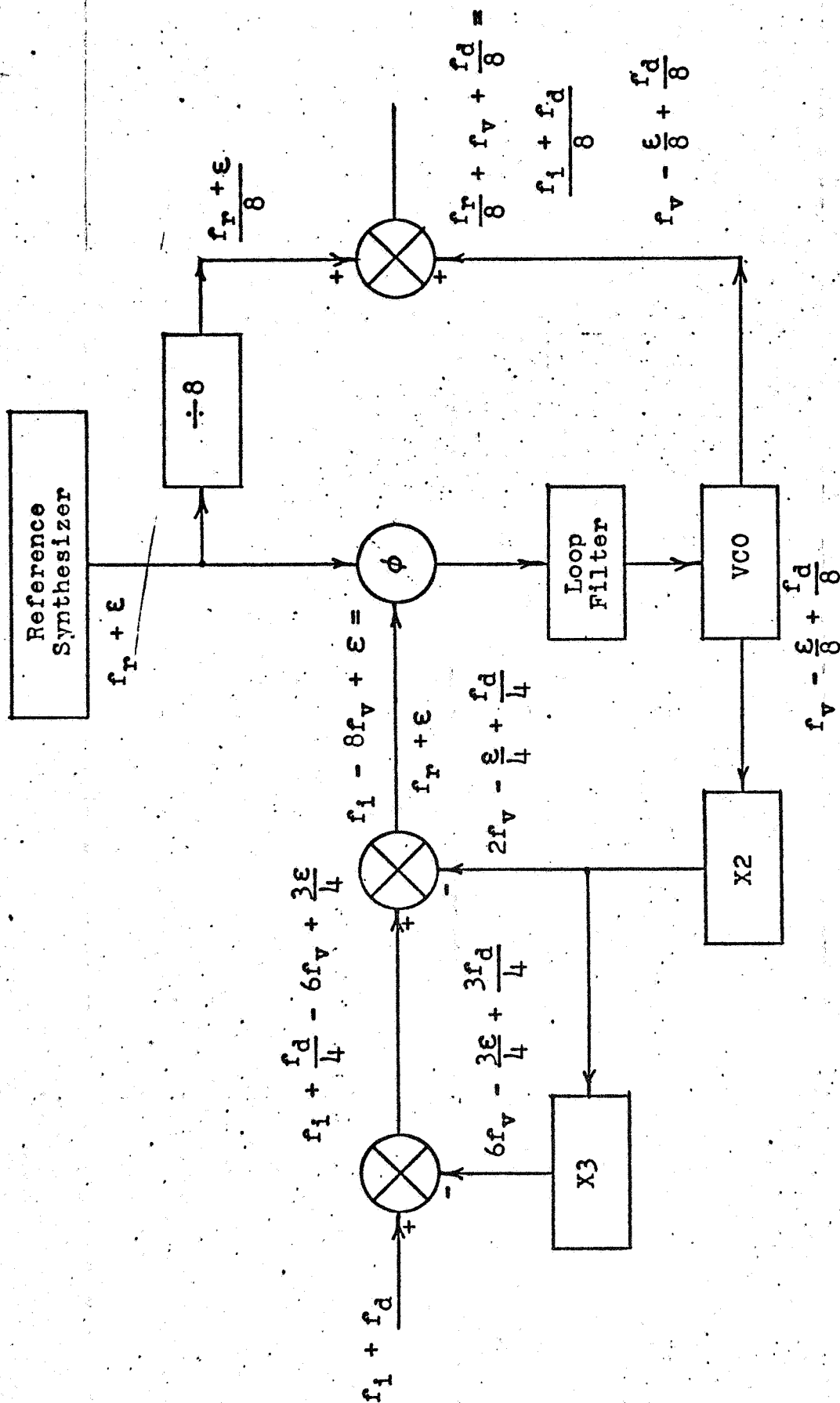
Figure 6-12 shows the frequency conversion loop of the Control Receiver and the first mixer of the Preset Synthesizer. The 9.6 MHz signal, used as a reference for the phase detector, contains a frequency offset, ϵ . When the carrier loop is locked, the local oscillator contains an error $\epsilon/8$ as shown in Figure 6-12.

In order to remove this frequency error, the 9.6 MHz reference is divided by 8 and added in a mixer to the VCO output. The errors cancel and the mixer output is:

$$\frac{f_r}{8} + f_v + \frac{f_D}{8} = \frac{f_i + f_D}{8}$$

This signal is shown as the reference input to the Preset Synthesizer (Figure 6-13). The 12.8 MHz VCO is phase locked to this reference.

The control receiver local oscillator may change frequency in steps of 3125 Hz as shown in paragraph 6.2.1.3. To accommodate these changes, digital programmable dividers are employed to



f_i = VHF input frequency
 f_d = Doppler offset
 f_v = Local oscillator frequency
 f_r = Reference frequency
 ϵ = Reference frequency error

Figure 6-12. Extraction of Reference and Reference Error

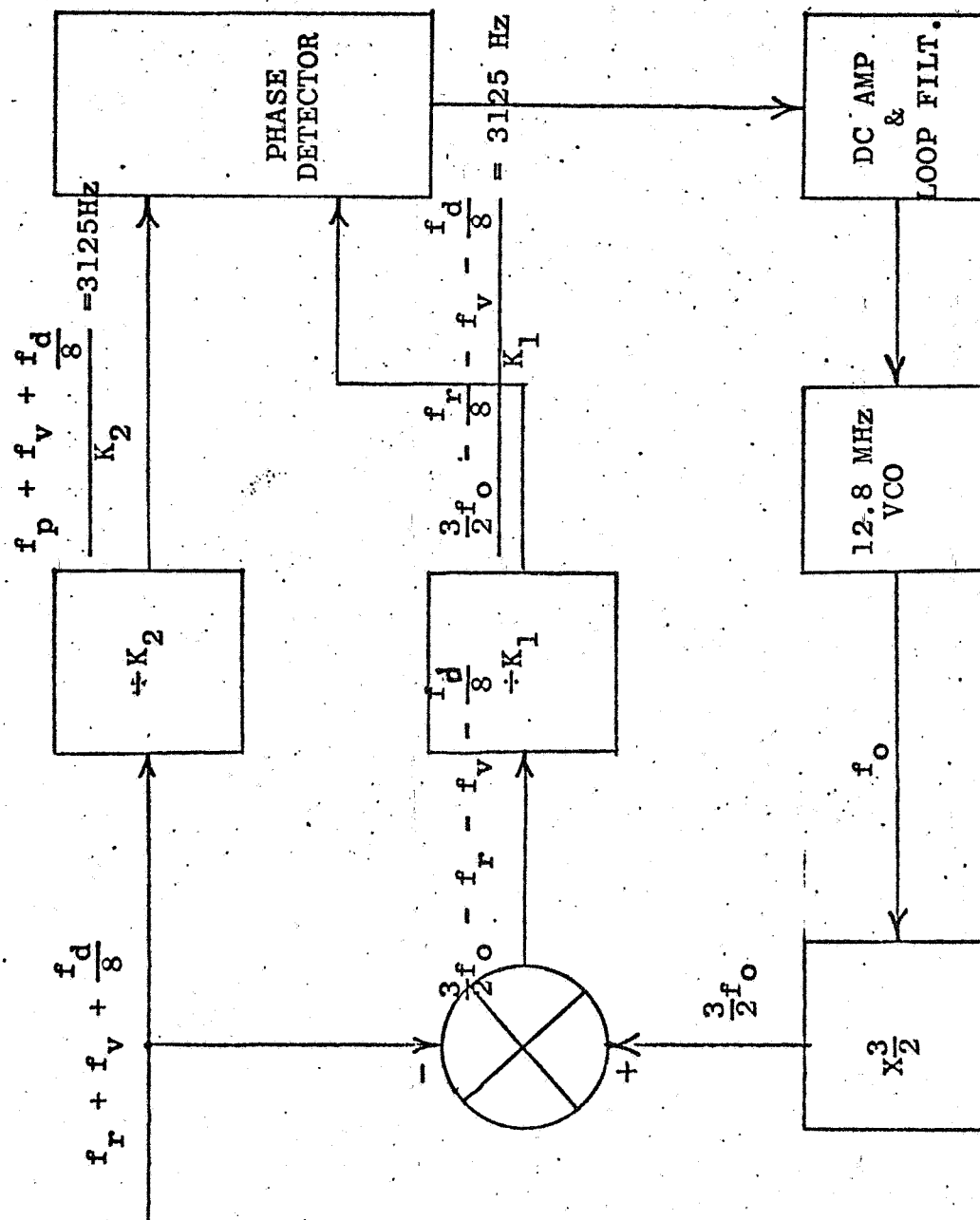


Figure 6-13. Preset Synthesizer Functional Block Diagram

provide fixed 3125 Hz signals to the phase detector. The frequency relationships of the loop are shown in Figure 6-13. Since the inputs to the detector are coherent, the following equation holds

$$\frac{\frac{f_r}{8} + f_v + \frac{f_D}{8}}{K_2} = \frac{\frac{3}{2} f_o - \frac{f_r}{8} - f_v - \frac{f_D}{8}}{K_1}$$

where: $f_o = 12.8$ MHz

$f_r = 9.6$ MHz

$f_v =$ Control Receiver local oscillator

$f_D =$ Doppler

To define K_1 and K_2 , assume f'_v to be center frequency of receiver oscillator with no Doppler present. Then:

$$K_1 = \frac{\frac{3}{2} f_o - \frac{f_r}{8} - f'_v}{3125} = \frac{18 \times 10^6 - f'_v}{3125}$$

$$K_2 = \frac{\frac{f_r}{8} + f_v}{3125} = \frac{1.2 \times 10^6 + f'_v}{3125}$$

For $f'_v = 16.05$ MHz

$$K_1 = \frac{1.95 \times 10^6}{3125} = 624$$

$$K_2 = \frac{17.25 \times 10^6}{3125} = 5520$$

Loop parameters are as follows:

$K_\phi = 7$ mv/degree

$K_v = 1$ kHz/volt

$A = 44$ volts/volt

Loop Bandwidth (β_L) = 15 Hz

6.2.2 Reference Synthesizer

The reference synthesizer provides coherent fixed frequencies to the transponder to be used for offset functions.

As shown in Figure 6-14, the synthesizer consists of a precision master oscillator operating at 3.2 MHz driving a combination of multipliers. Each multiplier is buffered for both its input and each output. The multipliers operate in a balanced configuration to give minimum coherent spurious output with non-critical filtering.

The 9.6 MHz outputs provide references for the control receiver phase detectors, the preset synthesizer first mixer, and an auxiliary output. The 8 MHz outputs provide frequency bias and phase detector drive in the tracking receiver. The 19.2 MHz output is used as a reference during Doppler reverse operation of the tracking transmitter.

6.3 CONTROL DATA DEMODULATOR

The Transponder Station Control Data Demodulator accepts the base band signal from the VHF Station Control Receiver, demodulates the binary data, and recovers the sub-bit timing reference. The serial binary data and the sub-bit clock are presented to the Station Control Logic, where the control instructions are decoded.

The function block diagram of the Data Demodulator is shown in Figure 6-15. The input signal is the three phase modulation of an 18.75 kHz subcarrier as described in specification 12-25607F. This signal has a strong component of the reference phase to which the subcarrier loop locks. The demodulated Return-to-Zero (RZ) signal is taken from the error point of this loop, multiplied by two, and the sub-bit timing frequency is recovered in the sub-bit loop. The sub-bit timing frequency or clock is used by the demodulator to recover the serial binary data with matched filter detection. A lock detector operating with the sub-bit sync is used to signal the Station Control Logic when the data are valid.

The Transponder Control Data Demodulator is located in the VHF Receiver drawer of the Transponder Equipment rack. The demodulator consists of two 6" x 6" printed circuit cards, 1A1A10 and 1A1A11 of the VHF Receiver drawer. A total of 270 discrete

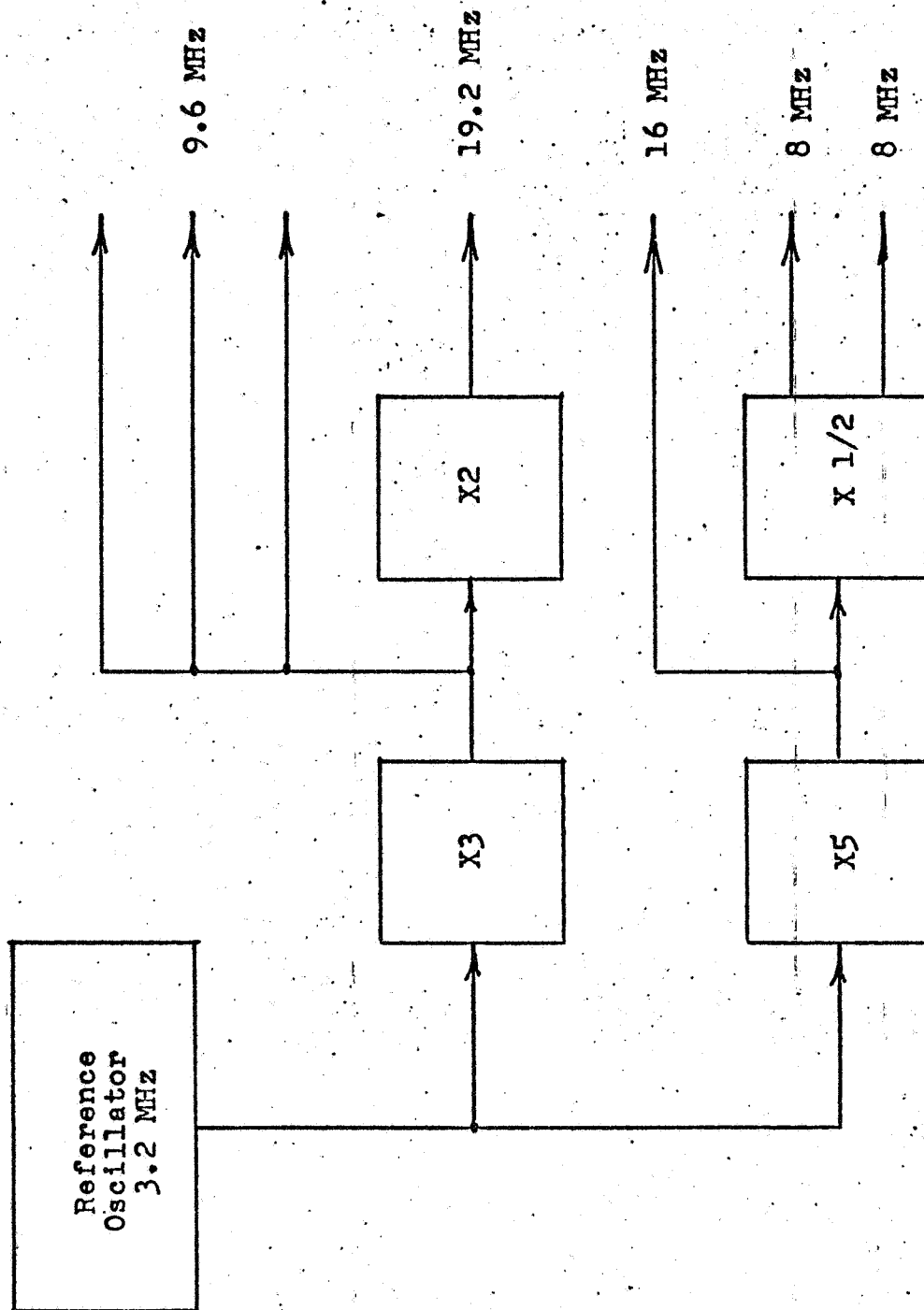
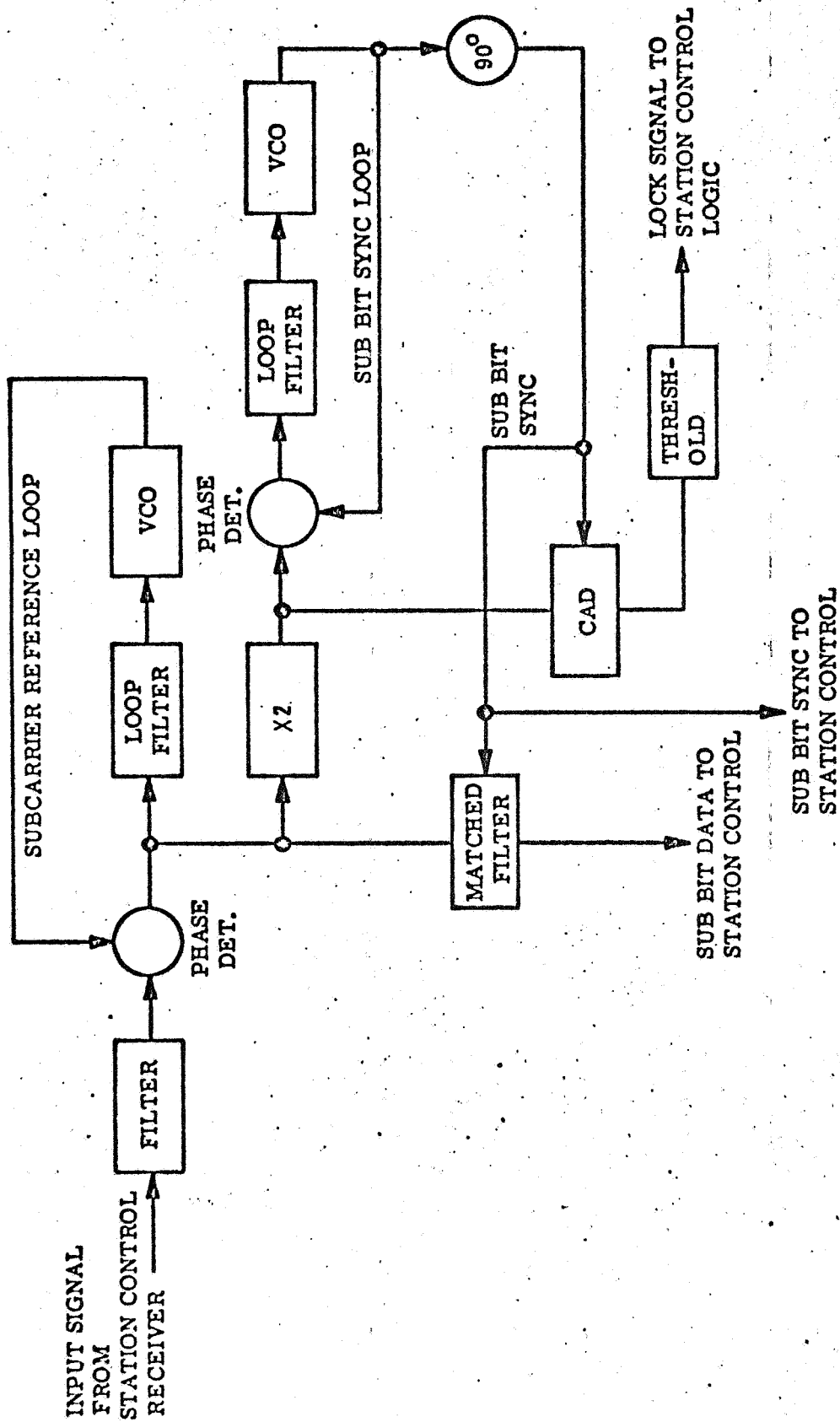


Figure 6-14. Reference Synthesizer



5259-23

Figure 6-15. Transponder Station Control Data Demodulator

components were used to implement the circuitry. Of these components, 25 are packaged in the three standard filter modules, 36 are packaged in the three phase detector reference driver modules, and 10 are packaged in the integrated circuit logic module which also contains the 11 integrated circuits that are used in the logic portion of the demodulator. The remaining components are mounted directly on the circuit boards. No effort was made to further reduce the size of the equipment because there was no space problem in the packaging scheme and no real advantage would be obtained at this point by building, at an increase in cost and labor, small quantities of specialized modules. In future applications, where size requirements or larger production quantities make the added expenditures feasible, the equipment would readily adapt to modular packaging, either cordwood or hybrid integrated circuitry.

The circuitry, which is largely digital in nature, requires a total power input of 1.12 watts. This is supplied as: 40 ma at 3.5 vdc, 50 ma at +9.0 vdc, and 55 ma at -9.0 vdc.

A block diagram of the Transponder Control Data Demodulator is presented in Figure 6-15. This is a basic diagram of the final implementation of the Demodulator. This section presents a discussion of the technical constraints that influenced the design of the various circuits that are used to implement the subsystem. The general factors that were considered are the various signal parameters, the signal conditioning required, the loop performance requirements, circuit implementation limitations and output signal specifications.

The Demodulator has the basic function of processing the VHF control data. The basic data rate is $F_L/16$ or approximately 780 Hz. In the Vehicle Equipment, the VHF data transitions are synchronized to the S-band range code transitions. The sub-bit sync ($F_L/16$) must be constructed such that the transitions of the Transponder sub-bit sync signal will correspond in time with those of the received range code transitions to within ± 40 microseconds.

This is an essential requirement for the presetting of the Transponder L-code. Static errors in the timing will be adjusted out of the VHF link by the Demodulator; but changes in these errors must be minimized, since they cannot be controlled. The best method of minimizing the effect of the changes is to minimize the total delay that must be removed. The subsystem must also provide the demodulated VHF control data to the Station Control Logic. The threshold error rate is defined as a probability of bit error of 4×10^{-5} . The rate at which the Demodulator acquires and begins to provide these signals was minimized to aid in rapid acquisition and reacquisition of the VHF link. The acquisition time was minimized wherever an unnecessary complication of circuitry did not result.

The 18.75 kHz subcarrier modulation is stripped from the VHF signal in the Station Control Receiver and presented from a 2000 ohm source impedance to the Control Data Demodulator. The signal content of this input is a phase modulated 18.75 kHz signal. The voltage level of this signal is 1.0 ± 0.2 volts rms. The noise voltage density at threshold is nominally 8 millivolts rms per Hz in a bandwidth of approximately 118,000 Hz.

A predetection filter is required to improve the signal-to-noise ratio (SNR) of the input signal. This reduces the dynamic range requirement for the subcarrier and sub-bit phase locked loops and allows a simplification of the associated circuitry. An excessive delay cannot be tolerated, however, since the variations in the delay result in an uncontrolled timing error in the sub-bit sync reference output. A noise bandwidth of 16 kHz was selected. This results in a threshold SNR of 0 db at the filter output.

A phase locked loop is locked to the filtered 18.75 kHz signal. The loop design parameters for the subcarrier reference loop are:

1. $2\beta_L = 100 \pm 10$ Hz
2. $\xi = 0.7 \pm 0.1$ at threshold
3. $K_V = 14,500$

The resulting performance parameters are:

1. Lock time, $t_L = 0.75$ seconds
2. Pull-in range = ± 300 Hz

This loop configuration is determined by a trade-off of circuit complexity versus lock time, phase jitter, and bandwidth. The demodulated RZ signal is taken from the error point of this loop and used to construct the sub-bit sync and data outputs.

The RZ signal is filtered in a simple R-C low pass filter, which is included in the X2 rectifier, to remove the 18.75 kHz switching transients. The filter has a cutoff frequency of 6.5 kHz and delays the signal by approximately 100 microseconds. This delay is less critical to the sub-bit timing because the delay removal capacitance can be made to accurately track the variations in the filter capacitance, the dominating factor in delay variations.

The filtered signal is then rectified in order to recover the sub-bit information. The resultant signal (RZ X2) is essentially the vehicle sub-bit sync signal as delayed by the VHF transmission path and signal processing. This signal becomes the input to the Sub-Bit Phase Locked Loop. The Sub-Bit Loop incorporates a VCO that operates at $F_L/4$ Hz. The VCO output is divided by four in a logic scheme that produces $F_L/16$, the output sub-bit sync signal, and the signals that are used to generate the loop reference signal and the data detection control signal. The loop has a built in timing offset that is used to cancel the VHF link delays in the reconstruction of the sub-bit sync timing.

The Sub-Bit Loop incorporates a $\pm 0.5\%$ VCO and a low offset phase detector to limit the frequency offset and allow for rapid acquisition. The loop design parameters are:

1. $2\beta_L = 35 \pm 5$ Hz
2. $\xi = 0.7 \pm 0.1$ at threshold
3. $K_V = 1200$

The resulting performance parameters are:

1. Lock time, $t_L = 0.055$ seconds
2. Pull-in range = ± 20 Hz

As in the subcarrier loop, the goal was acquisition speed, with minimum possible phase jitter and circuit complexity.

A lock indication signal is provided that is used in the Station Control Logic to verify the data quality. The rectified signal, RZ X2, is also used as the input to a CAD circuit, with $F_L/16$ being the reference signal. When acquisition occurs, a DC output occurs that is amplified and buffered by logic circuits to form the logic "one" lock indication signal.

In addition to being used to generate the sub-bit sync signal, the subcarrier loop error point signal, RZ, contains the VHF control data information. An integrate and dump match filter technique is used to extract the data. Figure 6-16 shows the timing of the integrate and dump process. The effective bandwidth of the decision circuitry is approximately 1600 Hz and the threshold SNR at the point of decision is approximately +10 db. The theoretical error rate at these conditions is one error per 10^5 bits. The control data is presented in complementary form to the Station Control Logic.

Figure 6-17 is a schematic diagram of the Transponder Station Control Data Demodulator. The logic elements shown are RTL circuits from the Philco MW3 logic family. This section presents brief circuit descriptions and some of the design considerations for these circuits.

6.3.1 Predetection Input Filter

The predetection filter is a three-pole bandpass filter. The center frequency is 18.76 kHz and the bandwidth is 15 kHz. The noise bandwidth is a maximum of 16 kHz. The nominal time delay of the filter is to be 35 ± 12 microseconds with variations due to environmental conditions to be less than 10% of the nominal. The

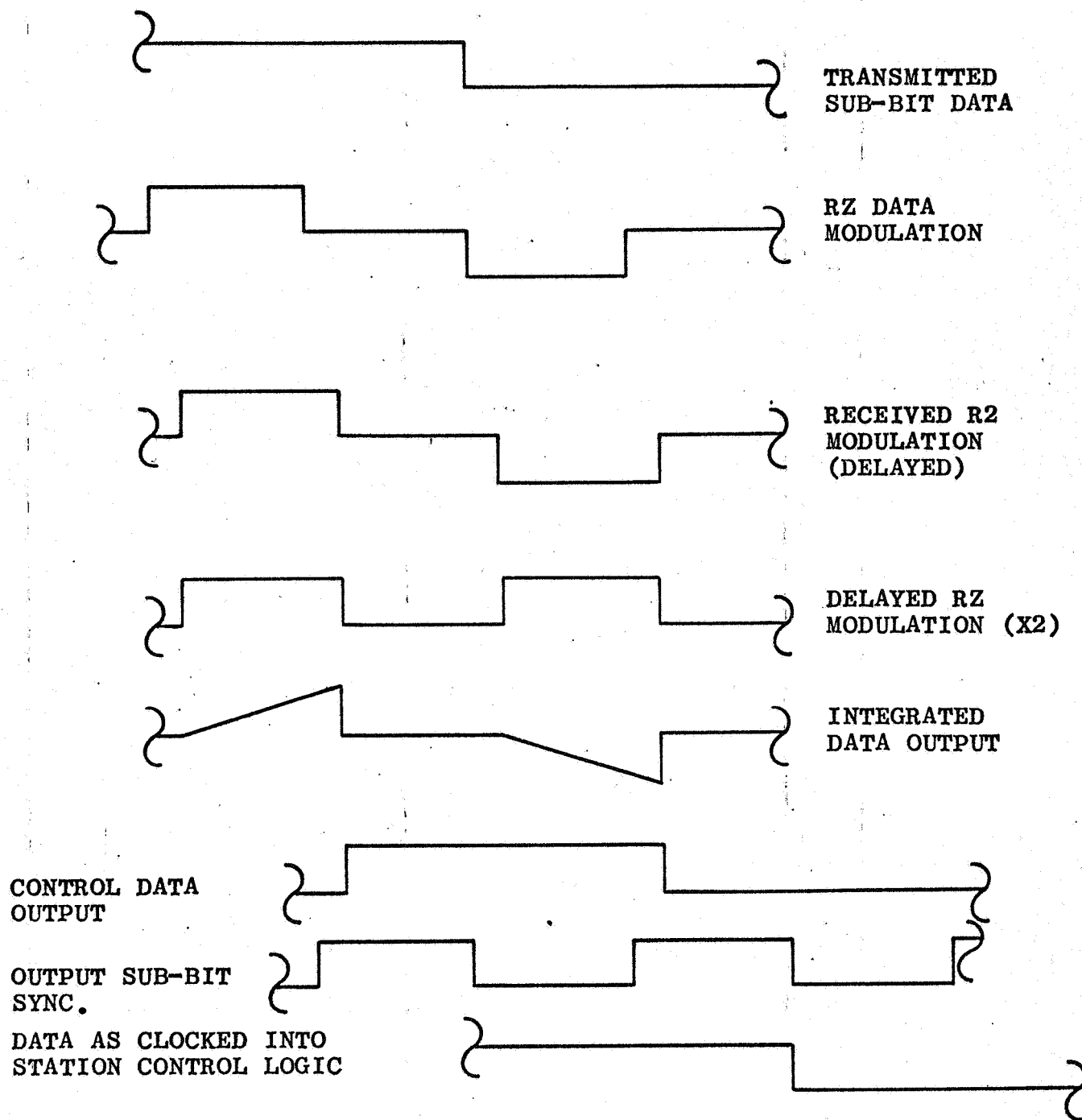


Figure 6-16. Timing Diagram of the Integrate and Dump Process.

input signal level is nominally 1 volt rms. The output of the filter is attenuated to 0.6 volts rms in order to limit the total dynamic range required in the phase detector.

6.3.2 Phase Detector Circuit

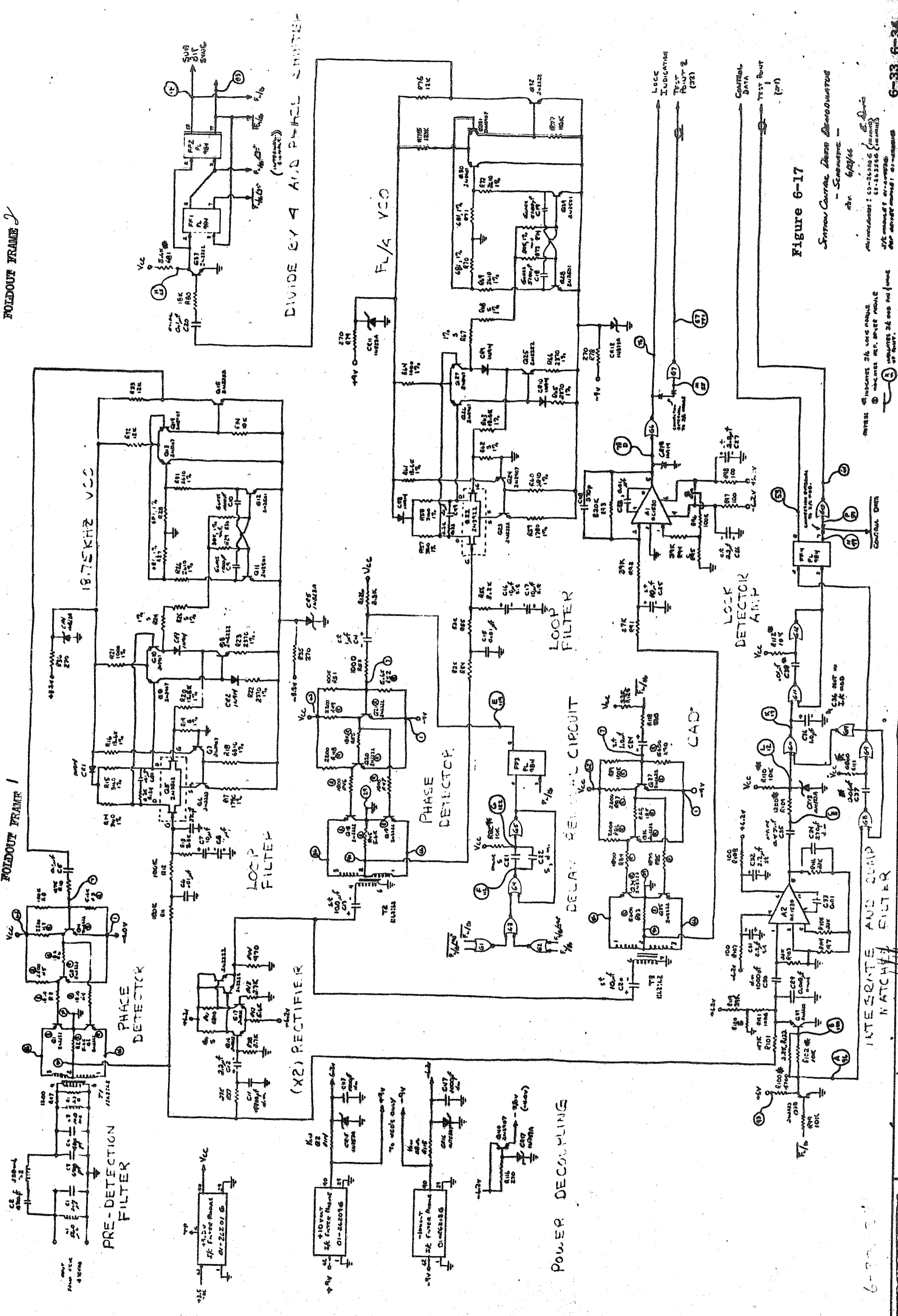
The phase detector circuit is used in both phase locked loops and as the CAD in the lock indicator circuitry. It is basically a pulse referenced, chopped phase detector. The reference pulse activates chopper transistors that alternately switch the phase of the center tapped transformer output. The circuit presents a 2000 ohm impedance to the input signal and an appropriate impedance to the reference source. The output is taken from the secondary center tap of the transformer and represents a 5.6 kilohm source impedance. The gain of the phase detector is a function of input level and will be further discussed in the following paragraphs.

The maximum input signal of the phase detector is ± 3.0 volts on the input terminals of the primary winding of the transformer. For signal levels above this level both positive and negative clipping will occur. This is largely negligible; however, for two reasons. First, the input signal will have only a small percentage of noise peaks that will exceed the dynamic range, which means that the clipping effect will be small. In addition, the positive and negative clipping is essentially balanced, which further reduces the offset voltage due to the dynamic limitations of the circuit.

6.3.3 VCO Circuit

An identical VCO configuration is used in both the subcarrier and sub-bit phase locked loops. Only frequency and gain determining component values differ between the two VCO circuits. The component reference designations that are used in the following discussion are those of the 18.75 kHz VCO in the subcarrier loop.

The VCO is a voltage controlled astable multivibrator. The control voltage as supplied by the loop filter is amplified in a



stable DC amplifier and used to vary the return voltage for the base timing resistors (R29 and R30) in the astable multivibrator. The input stage of the DC amplifier is a differential amplifier that incorporates field effect transistors (FETS) for high input impedance. A matched pair of FETS (Q5) is used for better temperature stability. The double ended output of the first stage drives a PNP differential amplifier second stage (Q9 and Q10). The feedback combination of R19 and R20 provides DC stability and gain control in the amplifier. R22, R23, and Q8 are biasing components for the output stage. CR1, CR2, and CR3 are temperature compensation diodes. The C50, R124 combination is a rolloff network that is used to prevent high frequency oscillation in the amplifier. Q7 is used to prevent the amplifier from operating until both power supplies are turned on. This is to avoid large initial frequency offsets at turn-on, which would otherwise occur if either power supply came on first. Other components are used for bias control and current limiting. The output control voltage is taken from the collector of Q10 and used to control the return voltage of the timing resistors in the multivibrator.

The astable multivibrator is formed by Q11, Q12 and the various bias resistors. The timing function is controlled by C9, C10, R29, R30, R24 and R25. The values of C9 and C10 are selected for the basic frequency of the VCO. Glass capacitors are used for good temperature stability. R29 and R30 are 33 kilohm metal film resistors, chosen for their temperature stability. R24 and R25 are selected components that are used to set the VCO frequency initially by adjusting the voltage that is supplied to R29 and R30 to the appropriate level. Q13, Q14 and Q15 are used as an isolation output amplifier, which provides the required output drive capabilities.

The VCO used +8.2 vdc and -8.3 vdc power sources. The supply voltages are zenered to ± 6.2 vdc, using 50 ppm temperature compensated zener diodes for thermal stability of the supply voltages. Each VCO requires 10 ma from each of the two power sources for a total power consumption of 160 mw in the VCO unit.

The VCO design is very stable. A frequency drift of only $\pm 0.3\%$ was measured over the temperature range from -25°C to $+85^{\circ}\text{C}$. The VCO gain in Hz/volt may be varied over a range from 0.2 to 1.0 times the center frequency with no change in the performance. The gain is stable to within $\pm 5\%$ over the entire temperature range. The circuit is versatile and can be used over a wide frequency range with minor changes in the circuitry.

6.3.4 The Subcarrier Reference Loop Design

This section is included as a summary of the design parameters for the subcarrier phase locked loop. This represents the final implementation of the loop and the final circuit design goals.

Loop Gain

The overall loop gain, K_V , is a composite of the phase detector gain, K_{ψ} , and the VCO gain, K_{VCO} . Neglecting the loss in the loop filter, which is less than 10% with the high input impedance VCO, the loop gain is:

$$K_V = K_{\psi} K_{VCO}$$

The gain of the phase detector is expressed as:

$$K_{\psi} = \frac{EP \text{ (input)}}{90^{\circ}}$$

For an input voltage of 0.6 volts rms, the value of K_{ψ} for the subcarrier loop is 10 mv per degree.

The value of K_{VCO} was set at 4000 Hz/volts, resulting in a loop gain, K_V , of 14,400 sec^{-1} .

Loop Filter Design

With the loop gain known, the values of τ_1 and τ_2 for the loop filter may be calculated for a given loop resonant frequency, ω_n . The subcarrier loop bandwidth, β_L , was set at 50 Hz. ω_n is then $8\beta_L/\sqrt{2}$ or 96 radians per second for a damping factor of 0.7.

The filter time constants are determined as follows:

$$\tau_1 = \frac{K_V^2}{\omega_n} = 1.53 \text{ seconds}$$

and

$$\tau_2 = \frac{\sqrt{2}}{\omega_n} = 0.0147 \text{ seconds}$$

An additional pole is inserted in the loop at 650 Hz for the purpose of removing the phase detector switching transients.

Loop Performance

The loop acquisition time is expressed as:

$$t_L = \frac{(\Delta F)^2}{L^3} (4)$$

The total frequency deviation, ΔF , is 130 Hz. (40 Hz due to maximum phase detector offset and 90 Hz due to maximum frequency drifts in the VCO.) The resultant lock time for $\beta_L = 50$ Hz is 0.7 seconds.

The pull-in range of the loop is defined as:

$$R = \frac{1}{\pi} \sqrt{\omega_n^5 K_V}$$

The pull-in range of the subcarrier is in excess of 300 Hz. The limiting constraint upon the loop is imposed by the input signal, however. The modulation technique generates 400 Hz sidebands of the 18.75 kHz subcarrier, the first of which is only 1.2 db lower than the subcarrier. The frequency drifts must not exceed 200 Hz from the center frequency of 18.75 kHz or the loop will acquire the sideband. This will be no problem, however, since the maximum drift of the VCO is limited to 130 Hz.

6.3.5 (X2) Rectifier Circuit

The X2 rectifier is an AC coupled differential amplifier stage. The complementary outputs of the amplifier transistors are summed into a 500 ohm load through emitter follower driver stages. This

allows an effective AC source impedance of as low as 20 ohms, while maintaining a high load impedance on the differential amplifier transistors, Q16 and Q17. A voltage gain of 40 is inherent in the device. The subcarrier loop output is 0.5 volts peak-to-peak, the attenuation of the low pass filter on the input is approximately 16 to 1. The resultant output from the rectifier is a 1.2 volt peak-to-peak pulse waveform.

6.3.6 The Sub-Bit Loop Design

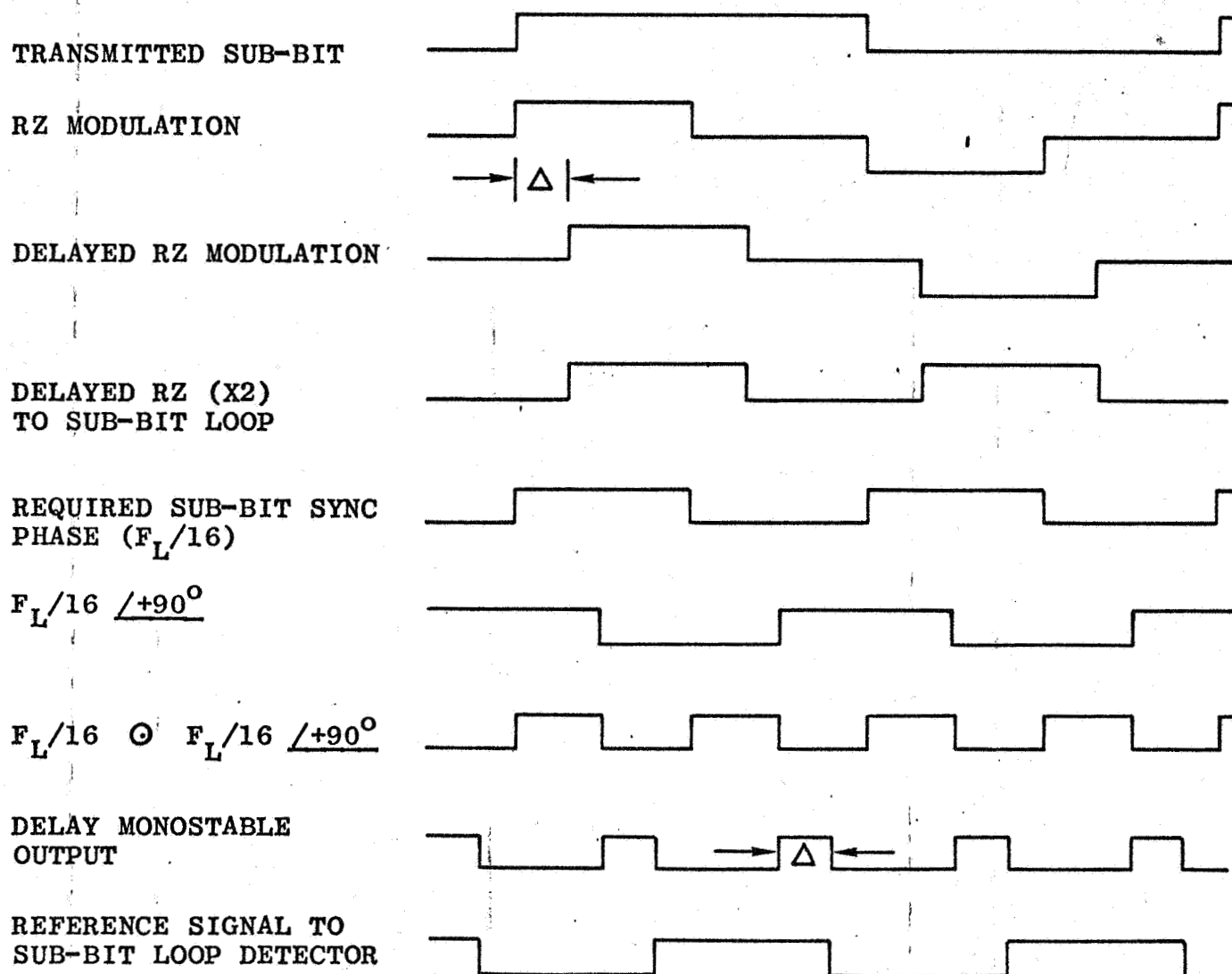
This section is included as a summary of the design parameters and special considerations for the sub-bit phase locked loop. This represents the final implementation of the loop and the final circuit design goals.

Divide by 4 and Phase Shifter

The VCO is operated at four times the input frequency to the loop. This is done primarily to simplify the loop. The VCO output, $F_L/4$, is divided by four to furnish the sub-bit sync, $F_L/16$, the data dump signal, $\overline{F_L/16}$, and the sub-bit loop reference signal as discussed below. The divide by four unit is a two-stage Gray Code counter. From such a counter, the $F_L/16$ signal, its complement and the $\pm 90^\circ$ phases of the $F_L/16$ signal may be obtained.

Delay Removal Unit

The function of this logic element is to produce the required reference signal for the sub-bit loop. The signal, $(F_L/16) (F_L/16 \angle +90^\circ) + (\overline{F_L/16}) (\overline{F_L/16} \angle +90^\circ)$, is formed in logic gating. This signal is inverted and drives a monostable multivibrator with an output pulse width equal to the total delay, Δ , that must be removed. This monostable output is used as the trigger pulse to shift the $F_L/16$ signal into a flip-flop. The output of this flip-flop is the reference signal $F_L/16$ delayed by 90° plus Δ , the required delay. The timing diagram of Figure 6-18 shows this procedure and the acquisition mode timing relationships.



NOTE THAT A $+90^\circ$ PHASE RELATIONSHIP EXISTS, BETWEEN THE LOOP INPUT SIGNAL AND THE REFERENCE SIGNAL, THE LOCK MODE CONDITION IS THEREBY SATISFIED.

Figure 6-18. Timing Diagram of the Sub-bit Timing Reconstruction Method.

Loop Design Parameters and Performance

Based upon the equations presented above, a summary of the sub-bit loop is as follows:

1. The phase detector gain, K_{ψ} , is 6.8 mv per degree
2. The VCO gain, K_{VCO} , is 1700/4 Hz per volt
3. The loop gain, K_V , is 1100 sec^{-1}
4. For β_L equal to 18, ω_n is 31.4 radians per second, τ_1 is 1.05 seconds and τ_2 is 0.037 seconds
5. The resultant lock time, t_L , is 0.055 seconds
6. The resultant pull-in range, R , is ± 20 Hz
7. The maximum frequency deviation, ΔF , is ± 8 Hz.

6.3.7 Lock Detection Indicator

The lock detection circuit incorporates a CAD, which is the phase detector circuit operated with a quadrature reference signal. The input to the loop is the RZ X2 signal output from the rectifier. The output of the CAD is heavily filtered to extract the DC component of the signal, which drives an inverting DC amplifier with a gain of 20. The output of the amplifier drives a logic gate that provides the lock indicator signal. The DC amplifier has an offset adjustment for adjusting the lock indication threshold. The output signal is a logic "one" when full lock is accomplished in the demodulator.

6.3.8 Integrate and Dump Circuit

The timing diagram of the data detection scheme was shown in Figure 6-16. The RZ signal, which contains encoded complementary data, is integrated in a long time constant integrator ($\tau = 3.2$ ms). The integration time is one-half the sub-bit period less the VHF link delay, approximately 600 microseconds. The signal $F_L/16$ is used to drive an inverting buffer that in turn drives the dumping transistor Q39, which essentially shorts the accumulated DC voltage on the integrator capacitor C29 to ground. The

voltage transition that occurs on C29 is coupled into a high gain amplifier ($A_v = 250$). The amplifier output is coupled into a threshold circuit (R110, G10 and CR13) where a logic "one" is generated from G10 if a data logic "one" was dumped. An inverted strobe pulse that was initiated by $F_L/16$ enables the data to be coupled to the steering input of a flip-flop, incorporating a monostable multivibrator to maintain the data information until the strobe pulse clocks it into the flip-flop. The complement of the data is presented to the Station Control Logic for use in system acquisition and control.

6.3.9 Power Supply Decoupling

All power lines are filtered with the standard AROD filter modules. In addition, zener regulation is used on both the ± 9 vdc power supplies wherever they are used in the demodulator. The heavy decoupling is used to reduce the spurious signals on the power lines to the lowest possible value, and to lessen the susceptibility of the demodulator to noise inputs.

6.3.10 Test Results

This section is intended to summarize the testing that was performed upon the Station Control Data Demodulator and to evaluate its performance with respect to the system requirements. Three such demodulators were built and tested for use in the AROD system.

In each unit, the VCO's, the phase detectors and the pre-detection filter were separately tested to determine their characteristics before they were combined into the subsystem. The VCO's of S/N 1 and S/N 2 showed a maximum frequency deviation of $\pm 0.3\%$ from the center frequency. Those of S/N 3 showed a maximum of $\pm 0.4\%$ deviation at the high temperature extreme. The VCO gain was generally stable from unit to unit. With only one exception, the maximum offset in any phase detector was 2 millivolts. The exception to this was the S/N 3 CAD, which measured as high as 9 millivolts at the high temperature extreme. The

filter characteristics were as predicted except for the delay, which was smaller than anticipated. The SN 3 filter was slightly more narrow in bandwidth, but this is not a problem. All measurements are within specified limits and the discrepancy itself may be traced to component tolerances and measurement error.

The phase locked loops were then tested, according to the test procedure. The phase response of each loop was measured. The first two units matched the theoretical response. The third subsystem loop responses indicated more narrow bandwidths than theoretically predicted by 10-15%. This error is not significant and will not appreciably affect the performance of the demodulator.

The third phase of testing consisted of acquisition and data error measurement tests on the demodulator. If frequency deviations are small, the unit will acquire at 5 db below the intended threshold. The lock indication when the unit has acquired is reliable to 4 db below the intended threshold and no false "locked" indication is generated even with large noise levels imposed upon the demodulation input. At the specified threshold level, the subcarrier was forced to acquire with signal frequency deviations of ± 100 Hz in the 18.75 kHz subcarrier over all environmental conditions. The low tolerance is lessened by 50 Hz at -25°C because of the effect of increased offsets in the phase detector due to clipping of noise peaks. Such offsets drive the VCO higher in frequency and force the unit to acquire with a large frequency offset. In every instance, however, 18.75 kHz was acquired. Similarly, the sub-bit loop acquired with offsets of ± 15 Hz. In each case, acquisition was not "worst case". The numbers given represent "quick-acquisition" limits, not extremes or absolute limits in range.

The error rate was in line with predicted levels. At $+25^{\circ}\text{C}$, the probability of bit error was 1.5 to 2.5×10^{-5} at the defined threshold. This is approximately 0.5 to 1.0 db below theoretical in actual threshold level. The error is attributed to phase

offset in the matched filter, phase jitter in the sub-bit sync signal and test equipment accuracy limitations.

The sub-bit sync timing is reconstructed to within 20 microseconds with a maximum peak jitter of 80 microseconds at threshold. This represents the performance over the entire thermal environmental range. The errors are larger than the design goal, but the system analyst has verified that the demodulator should still perform adequately in the presetting of the transponder L-code.

The demodulator required 1.12 watts of power. This is supplied as follows:

+9.0 vdc at 52 ma

+3.5 vdc at 42 ma

-9.0 vdc at 56 ma

This is within the constraints of the specified goals.

The Control Data Demodulator is technically sound. The demodulator performs all of the required functions and will acquire in a minimal time. It is realized that a large circuitry requirement exists. This is a direct result of the complexity of deriving the data and supplying the associated signals with the required precision in timing that is required in presetting the code.

The phase detector has a limited dynamic range. This results in noise peak clipping and voltage offset in the phase detector output. This condition is only a problem at cold temperature extremes (-25°C) and will not be a problem in the transponder application because there is a temperature rise in the equipment above the ambient environmental conditions. Should future applications require the elimination of this effect, however, a new detector configuration or limiting of the input signal dynamics could be incorporated.

The equipment is built with a minimum of selected components. Component tolerances create performance deviations, but these are

minor and do not affect, in any significant way, the overall performance of the demodulator. The circuitry is not critical and will perform to the specifications imposed upon it by the requirements of the AROD system.

6.4 STATION CONTROL LOGIC

The station control logic directs the sequence of operations of the transponder station. It decodes, verifies, and operates on the VHF data from the vehicle to provide the necessary signals to other transponder subsystems. The station control logic also generates and formats the S-band data to be transmitted to the vehicle via the S-band link.

When the transponder station is in the TRACK mode, the S-band transmission link may be used to transmit external data, such as a complete new program of memory data, to the vehicle. Input gates and clock pulses are provided for this purpose. However, external equipment must be used to encode and generate the required S-band transmission data and control codes.

The station control logic is designed to respond to four different site ID's, i.e., to simulate four transponder stations. The four site ID codes are purposely arranged in such a manner that four of the six bits of the ID codes are common among the four site ID's. Any combination of these four bits may be selected by a bank of ID switches. The remaining two bits identify the individual site ID. The priority of the four site ID's is arranged on a first-come-first-serve basis. Once a given site ID is detected and verified a priority signal is generated to inhibit the verification of all other site ID's. The control logic for the detection and verification of three of the four site ID's is packaged in one micro-harness module so that the transponder station may be readily modified to respond to only one site ID.

6.4.1 Detailed Functional Description

The transponder station control logic consists of eight micro-harness modules. All these modules are housed in one mother board. A simplified functional block diagram of the station control logic is given in Figure 6-20. The functional blocks enclosed by the dashed line are used only in the test model transponder station to simulate four transponder stations at one test site.

VHF Data Flow

A major portion of the station control logic is used to control the flow of the VHF data. The data flow diagram is given in Figure 6-21. The station control logic is normally at the standby mode until the Data Channel Lock signal from the VHF demodulator becomes a ONE. The demodulated sub-bit data are then serially shifted into the input data register at the sub-bit rate until a sync word (111000) is detected. The detection of the sync word sets the station control logic to its operational routine. If the next two sub-bits following the sync word represent the event marker, which indicated the beginning of a major frame of VHF data, the combination of the event marker and sync word is used to turn on the main power for other subsystems. The transponder station enters the standby mode. This combined signal is also used to start the 16-frame counter, reset the 5-minute timer and preset the L-code in the Code Control subsystem.

Once a word sync is detected, regardless of the status of the event marker data bit, the station control timing generator is initiated to generate the necessary timing pulses to decode and verify the VHF data. The VHF data format is given in Figure 6-22.

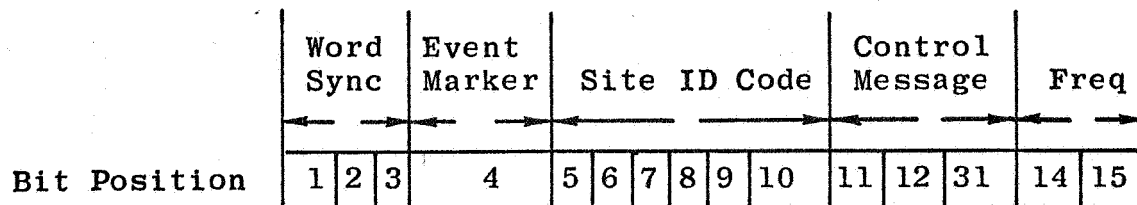


Figure 6-22. VHF Data Format

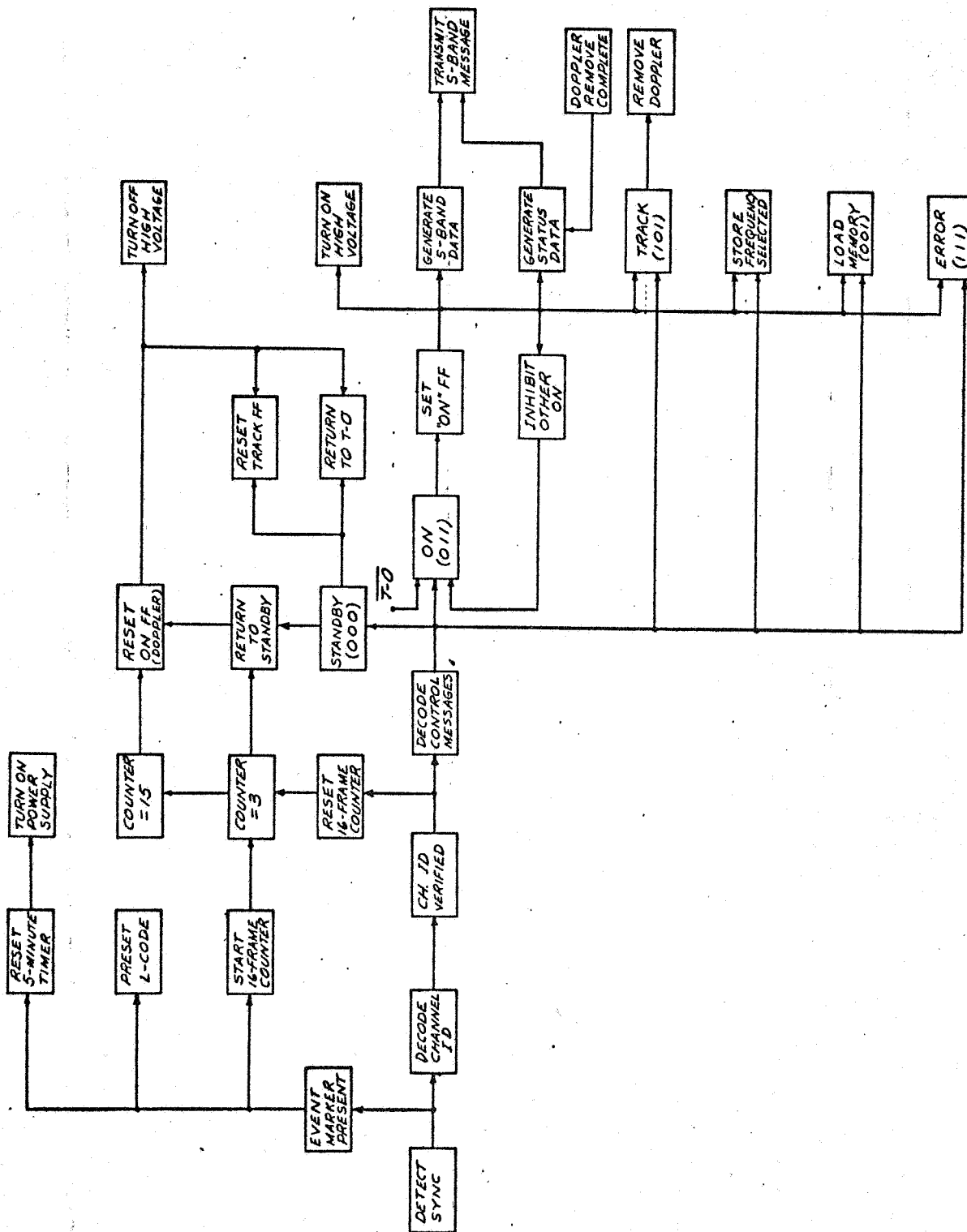


Figure 6-21. AROD Station Control Logic VHF Data Flow Diagram

All VHF sub-bit data following the event marker, data bit #4, are decoded. If the site ID code, data bits #5 through #10, is verified, the control message and frequency data are strobed into the pertinent registers. If the site ID is not verified, the control message and frequency data are inhibited until the next minor frame. The decoding and verification operation continues as long as word sync is detected. However, if no site ID is verified after 16 major frames, approximately 2.5 seconds, the output of the 16-frame counter resets the various control message flip-flops and signals the code control sub-system to return to state T-0. This particular reset operation is not a necessity at this time but only as a convenience. A detailed description of the 16-frame counter may be found in Section 6.4.2.

When the site ID code is verified, the control message data are routed to the control message detector, and the frequency data are shifted into the frequency storage register flip-flops. The control message detector is arranged in such a manner that the first control message so detected must be the ON (011) control message. When the ON control message is detected, the ON flip-flop is set to enable the detection of all other control messages. The ON flip-flop also enables the transmitter to transmit S-band data to the vehicle. The station control logic retains its status quo until other control messages are detected. When the TRACK (101) control message is detected, the station control logic signals to remove negative doppler. After the negative doppler is completely removed, the station control logic changes the 2nd sub-bit of the station status data from a ONE to a ZERO and transmits this bit of information to the vehicle via the S-band link. The transponder station is then considered to be acquired.

To release the transponder station, the vehicle must originate the RETURN TO STANDBY (000) control message. When such a message is detected, the station control logic immediately disables the S-band transmission link and resets the TRACK flip-flop. The RETURN TO STANDBY message is stored in the RTS flip-flop for the

next three major frames. If the previously selected site ID code reappears during this interval, the station control logic uses the stored RETURN TO STANDBY control message as the condition to reacquire the VHF signal. However, if the previously selected site ID code does not reappear by the beginning of the third major frame after the RETURN TO STANDBY control message is received, all ON flip-flops are reset at P5 time to enable the transponder station to select the appropriate new site ID.

Test Model

The station control logic is designed to simulate four transponder stations and responds to four different site ID's. The functional blocks for the simulation logic are enclosed by the dashed lines in Figure 6-20. This portion of the logic is packaged in one micro-harness module, such that the station control logic may be readily modified to respond to only one site ID with minimal redesign efforts.

Four site ID detectors are shown in Figure 6-20. They are labeled as site ID detector X0, X1, X2 and X3, where X represents the four higher order bits of the site ID code while 0, 1, 2, and 3 are the decimal equivalent of the two low order bits. The four high order bits of the site ID code for a particular transponder station are determined by the settings of the site ID switches mounted on the front panel. The two low order bits are pre-wired. It is obvious that the four site ID codes associated with the particular transponder station differ from each other by two bits at the very most.

A single ON control message detector is used to control the output of the four site ID detectors. When the Code Control is in state T-0, the ON detector is inhibited. When the Code Control is not in state T-0, the ON detector output is logically combined with the outputs of the site ID detectors and the priority determinator to select the appropriate ON flip-flop. When the priority determinator is not assigned to any particular channel, the first correctly received site ID control and the associated ON control

message are gated through the ON control logic to set the pertinent ON flip-flop. The output of the selected ON flip-flop sets the priority determinator to select and operate only on that portion of the input data which are associated with the selected site ID.

Normally the RETURN TO STANDBY control message reverts the transponder station to the standby mode. However, such an action causes complications in the test model. If the RETURN TO STANDBY control message is due to a drop-out, channel priority must be retained so as to reacquire the same signal. On the other hand if the RETURN TO STANDBY is due to maximum range, the priority determinator must revert to first-come-first-serve operation. The station control logic is designed to treat the RETURN TO STANDBY control message as if it were due to a drop-out until further clarification is received from the vehicle.

When the RETURN TO STANDBY control message is received, the station control logic resets the various control message storage flip-flops, instructs the Code Control to return to state T-0, and disables the S-band transmission link. The information stored in the priority determinator is retained for the next three major frames. If the previously selected site ID reappears during this interval, i.e., the RETURN TO STANDBY control message is due to a drop-out, the station control logic proceeds to operate on the reacquired signal. If the previously selected site ID has not reappeared by the third major frame, the priority determinator is then reset to accept other site ID's.

S-Band Data Format

The S-band data are transmitted to the vehicle in a 10-bit data format as shown in Figure 6-23. The first 3 bits (6 sub-bits) are used as word sync, which is represented by the sub-bit pattern 111000. Bits 4 through 9 are the site ID code. The last bit transmits the station status. The significance of the two station status sub-bits is given in Table 6-4. The first sub-bit represents the status of T-A_H and the second sub-bit represents that of the doppler-reverse-complete (T-DRC).

| | | | | | | | | | |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|-----------------|
| t ₁ | t ₂ | t ₃ | t ₄ | t ₅ | t ₆ | t ₇ | t ₈ | t ₉ | t ₁₀ |
| Sync | | | Site ID | | | | | | Status |

Figure 6-23. S-Band Data Format

The S-band data rate is approximately 50 bits per second. Each data bit is encoded into two sub-bits. A ONE in the site ID data is encoded into a ZERO followed by a ONE, while a ZERO is encoded into a ONE followed by a ZERO. The resulting transmission rate is approximately 100 sub-bits per second.

TABLE 6-4. Station Status

| Status | | Bit 10 | |
|------------------|-------|-------------|-------------|
| T-A _H | T-DRC | 1st Sub Bit | 2nd Sub Bit |
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 |

6.4.2 Station Control Logic Implementation

This portion of the report contains a detailed description of the logic diagrams of the station control logic. The drawings referred to are detailed logic diagrams and are quite bulky; therefore, they are not distributed to the entire distribution list. These drawings are furnished only upon request. It must be pointed out that these logic drawings are production drawings which may be modified slightly during the remainder of the program.

VHF Timing Module

The VHF sub-bit sync pulses are used to generate the necessary timing pulses to operate on the received VHF data. The logic for generating these timing pulses is shown in the VHF Timing Module, logic diagram #69-24440G.

The VHF sub-bit sync, which is a train of pulses, is gated through G20, G21, G9 and D2. The output of D2, labeled $2CL_{VHF}$, is used to trigger the appropriate flip-flops directly. Gates G20, G21, and G9 are used to equalize the delay so that the output of these gates may be properly controlled. For example, the trigger input to FF3 goes through same number of gates and driver as that of FF2 in relation to the VHF sub-bit sync, even though the two trigger pulses come from different paths.

FF3 is connected as simple binary counter, which divides $2CL_{VHF}$ by 2 to obtain CL_{VHF} and $\overline{CL_{VHF}}$. Word sync is gated through G15 to reset FF3 so that CL_{VHF} can always correctly decode the sub-bit data following word sync. The sync pulse also sets FF2 and resets FF1 and the ripple counter, FF4, FF5, FF6, and FF7. The state of the counter is always 0 immediately following the trailing edge of the sync pulse, and starts to count CL_{VHF} pulses through gates G16, G18, and G12. At a count of 5 (0101) the negation output of G22 attempts to transfer the site ID data from the input data register into the ID data register. The actual transfer is executed only if the transponder station priority has not been assigned. In the meantime the received site ID data are compared with the four site ID stored in the transponder station.

When the counter reaches a count of 1010 (decimal 10), the output of G7 is gated with $2\overline{CL_{VHF}}(2)$ to reset FF2. The ZERO output of FF2 inhibits G13 and G16 while the ONE output enables G17 to change the input to the counter from the CL_{VHF} rate to that of $2CL_{VHF}$. Finally at the 14th (1110) count the output G6 enables G1 to set FF1, which inhibits G17. The counter stops counting until the next word sync is detected. The relationship between the various timing pulses is given in Figure 5.

Input Data Register Module

The Input Data Register Module (69-24436G) accepts the sub-bit data from the VHF Data Demodulator when the Data Channel Lock signal is a ONE. If the channel is not locked to the vehicle, only ZERO's are shifted into the data register flip-flops.

Sub-bit data are shifted into a 2-stage shift register, flip-flops FF3 and FF2. The contents of the two flip-flops are mod-2 added in A1 to check for parity errors. Only those that are coincident with CL_{VHF} are stored in FF1. Word sync (111000) always generates two such errors. Therefore, it is necessary to reset FF1 with the sync pulse prior to the arrival of the site ID data.

FF3 and FF4 through FF10 form an 8-stage shift register. The shift clock to FF3 is fixed at the sub-bit data rate, $2CL_{VHF}$, and that of FF4 through FF10 varies with function of the shift register, either at $2CL_{VHF}$ to detect word sync or at CL_{VHF} to store data. The two inputs to D1 come from the VHF Timing Module. When the system is searching for word sync, the DATA \overline{CL} input is low, which enables $2\overline{CL_{VHF}}(3)$ through D1 to shift FF4 through FF10 at the same rate as FF3. When a sync word is detected, DATA \overline{CL} becomes a square wave, which effectively changes the output of D1 from $2CL_{VHF}$ to CL_{VHF} for the next eleven data bits. This is the procedure employed for decoding the site ID, control message, and frequency data from the sub-bit data. If no parity error is stored in FF1, $\overline{P5}$ is gated through G18 in an attempt to transfer, in parallel, the site ID data stored in FF3

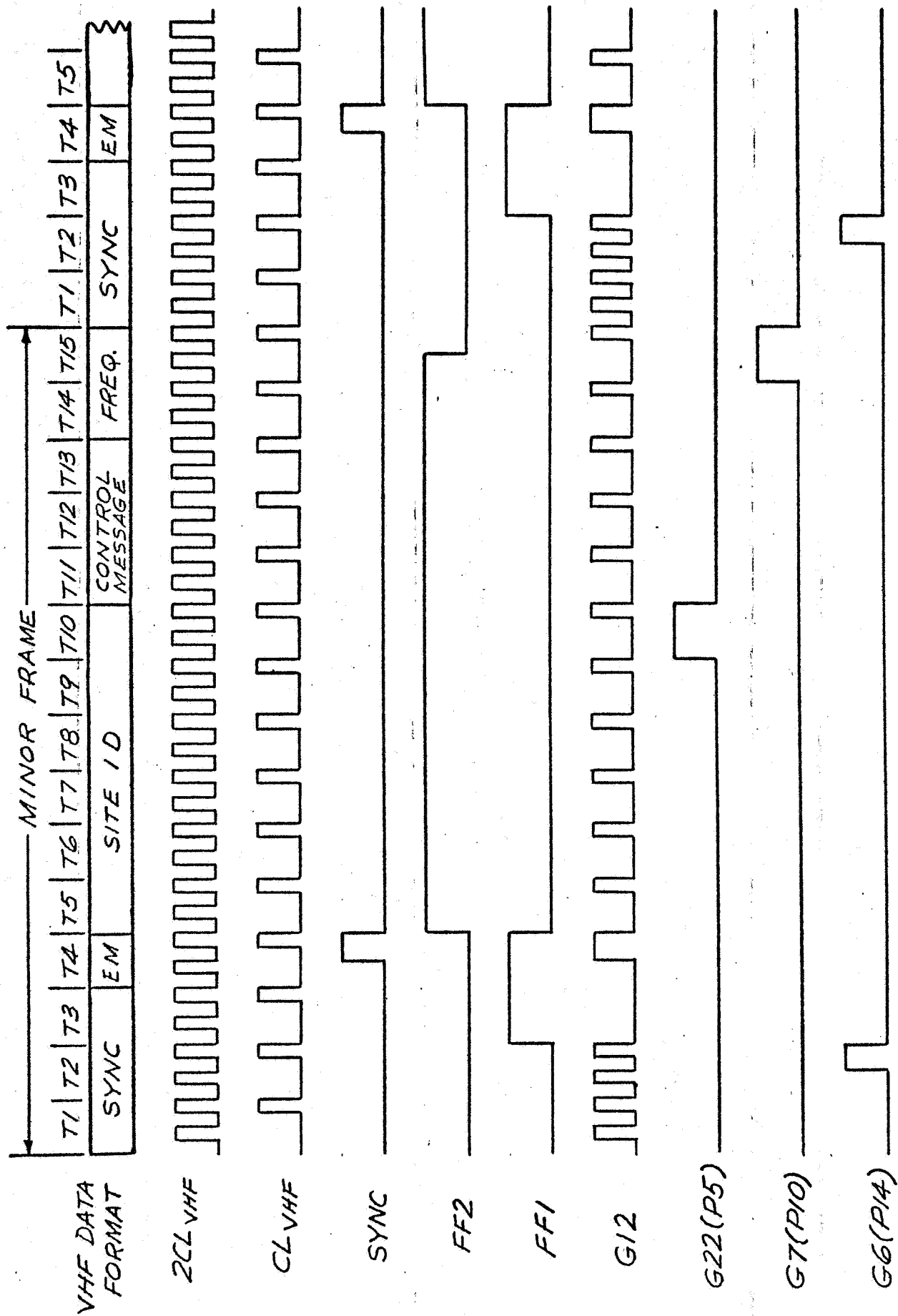


Figure 6-24. VHF Timing Diagram

through FF8 into the ID Data Register, as described in 3.1. The control message and frequency data are decoded 5 bits later at P10 by the Control Message Detector module.

The TRANSMIT ENABLE signal (output of G16) is part of the site ID priority determination logic. Its operation is more closely related to that of Logic Module A and Logic Module B.

ID Data Register Module

The ID Data Register Module (69-24432G) consists of the word sync detector and a 6-bit shift register and its control gates. The shift register accepts the 6-bit site ID data in parallel from the Input Data Register when the transponder station priority has not been assigned. It also stores and recirculates the selected site ID for the S-band Data Encoder.

The shift register, FF1 through FF6, is controlled primarily by two signals, SELECTED ON and TRANSMIT ENABLE. These two signals are closely related to each other, and are defined in Section 3.5. The SELECTED ON signal controls the data drop-in gates G3, G7, G10, G13, G17, G20 and G22, while TRANSMIT ENABLE indirectly controls G4, G5, G8, G11, G14, G18 and G21. Only one set of gates can be selected at a time, however both can be inhibited simultaneously. When SELECTED ON is a ZERO, TRANSMIT ENABLE is necessarily a ZERO, the data drop-in gates are enabled to accept site ID data from the Input Data Register. The data lines are labeled as FFA, FFB, FFC(2), FFD(2), FFE(2), and FFF, where FFA is the high order bit and FFF the low order bit. These data are strobed into the shift register once per minor frame by ID STROBE through G22 until the proper site ID is selected. The SELECTED ON signal then becomes a ONE and inhibits the data drop-in gates. When TRANSMIT ENABLE becomes a ONE, the output of D2 enables the other set of gates to recirculate the selected site ID data under the control of the S-band logic at G21.

The combination of G25 and G26 is arranged to detect word sync, 111000. Output pin #9 of G26 is gated with FFB and \overline{FFA} at G23 to detect the event marker, such that G23 is effectively detecting an 8-sub-bit code of 11100001. The output of G23 is labeled PRESET and that of G16 \overline{PRESET} . Each PRESET pulse represents a major frame. The \overline{PRESET} pulse is used by the Code Control Subsystem to preset the L-code as required.

Control Message Detector Module

The Control Message Detector Module, #69-24428G, decodes the various control messages and stores the frequency code and other pertinent data.

Flip-flop FF1 stores one of the four site ID's associated with transponder station. Gate G25 detects site ID code XXXX00. The XXXX portion of the code is labeled as ID ENABLE (pin #6 of G25). It represents the four high order bits of the ID code and is selected by setting the ID switches to the right combination. The output of G25 is shifted into FF1 by the ID STROBE pulse at P5. The ZERO output of FF1 enables G1 to store the ON control message in the ON flip-flop in Logic Module A at P10 if there is no parity error and station priority assignment. If the station priority has been assigned to a given ID code the output of G1 is inhibited in Logic Module A.

The 2-bit frequency data are stored in flip-flops FF2 and FF3. Data are strobed into these two flip-flops once per minor frame at P10 until a site ID is selected. After the station priority has been assigned to the selected site ID, only the ON PULSE is allowed to shift the frequency data into FF2 and FF3. This particular implementation is necessary in order to take care of the case where the first proper site ID code is received correctly while the ON control message and/or the frequency data have one or more bits in error. Gates G8, G11, G14, and G16 decodes the frequency data to provide four channel frequency output lines. The channel frequency assignments are given in Table 6-5. The four output lines, output of D1, D2, D3, and D4, are normally ZERO

TABLE 6-5. Channel Frequency Assignment

| Channel | FF3 | FF2 |
|---------|-----|-----|
| A | 0 | 0 |
| B | 1 | 1 |
| C | 1 | 0 |
| D | 0 | 1 |

(low) until all data are correctly received. The select channel frequency line becomes a ONE as the TRANSMIT ENABLE signal becomes a ZERO. Three additional outputs, P_0 , P_1 , and P_2 are provided for the divide by k logic in the Divider, Synthesizer Loop for proper frequency generation.

The ON control message is decoded by G28. When the Code Control is not in state T-0, G28 always detects the 3-bit combination of 001 (high order bit first). However, the output of G28 is significant only at P10. The right code occurring at the wrong time is inhibited. The decoding of the other control messages is deferred until a site ID and its ON control message are correctly received. Gates G26 and G27 are arranged to decode 1X1 and 00X respectively and are controlled by the $\overline{\text{ON PULSE}}$. The inverse of G26, $\overline{1X1}$, is combined with $\overline{\text{FFD}}$ at G18 to detect 111, which indicates that the new program data loaded into the vehicle memory contain parity error(s). Similarly G20, G21, and G23 decode respectively the TRACK (101), RETURN TO STANDBY (000), and LOAD MEMORY (001) control messages.

Flip-flop FF4 is a simple binary counter which divides $L_{59} + L_{127}$ by 2 to generate the S-band clock CL_{SB} and $\overline{\text{CL}_{\text{SB}}}$ for the Encoder Module.

Logic Module A and Module B

Logic Module A (69-24420G) and Logic Module B (69-24424G) control the basic sequence of operation. Logic Module B is required only in the test model to simulate and respond three additional

site ID's. The three site ID codes are: XXXX01, XXXX10, and XXXX11, where the high order bits are pre-selected by the site ID switch bank. The test model transponder station can be readily converted to a normal single site ID station by replacing Module B with interconnecting wires.

The ID ENABLE signal to Logic Module B is normally high. When the four high order bits of the site ID code match the settings of the XXXX position of the ID switch bank, the ID ENABLE signal becomes ZERO to enable G21, G22, and G23 to check the remaining two bits of the site ID code. G21 responds to 11, G22 to 10, and G23 to 01. The XXXX00 ID gate and storage flip-flops are located in the Control Message Detector module (see Section 3.4). The received site ID code is compared once per minor cycle with the four stored ID codes. Any match is shifted into the appropriate ID storage flip-flop, FF1, FF2, or FF3, by the ID STROBE pulse. (Site ID storage flip-flop for XXXX00 is located in the Control Message Detector module). Only one of these four flip-flops can be selected at any minor cycle. The flip-flop so selected enables the \overline{P}_{10} + ERROR pulse to sample the control message. If the control message is ON (011) the corresponding ON flip-flop, FF4, FF5, or FF6 of Module B or FF1 of Module A, is set to assign the station priority to the selected site ID. This is accomplished by combining the set output of the ON flip-flops in G27, Module B. The setting of the ON flip-flop changes the output of G27, SELECTED ON, from a normally ONE signal to a ZERO. Gates G24, G25, and G26 of Module B and G25 of Module A are inhibited by SELECTED ON, which effectively retains the ON control message in the pertinent ON flip-flop, while excluding the other three flip-flops from setting. The transponder station is considered locked to the selected channel and responds only to the control messages associated with that particular site ID.

The above description may be better illustrated by an example. Assume that the transponder station has been in the STANDBY mode

for sometime, and XXXX11 is the first correctly received site ID code. Gate G21 of Module B conditions ID storage flip-flop FF1 to be set by the ID STROBE pulse, while simultaneously resetting the other three ID storage flip-flops. If the next 5 data bits, which must be the ON (011) control message and frequency code, are correctly received; i.e., no parity error, the $\overline{P_{10}}$ + ERROR signal is passed through G6 to set FF4. Setting FF4 to a ONE forces output pin #8 of G27 to be a ZERO. The SELECTED ON signal is routed to G16 of the Input Data Register module, 69-24436G, and to D2 of the 5-minute timer module, 69-24473G. The output of G16 is used to enable the ID Data Register to recirculate the ID Data as needed, and to identify the selected channel frequency. The output of D2, which is labeled SELECTED ON, inhibits the ID strobe and data drop-in gates in the ID Data Register and the ON control gates, G25 of Module A and G24, G25, and G26 of Module B, thus ignoring all subsequent ON control messages. The ONE stored in FF4 automatically assigns the station priority to site ID code XXXX11. The transponder station ignores all other site ID codes and responds only to the control messages associated with the selected site ID, excluding the ON control message. These control messages are sampled only once per major cycle by ON PULSE, which is generated by combining the output of G8 and FF4 at G12. If the selected site ID and/or its control message data are received with parity error, no ON PULSE signal is generated. When the TRACK control message is detected, it is stored in flip-flop FF6 which initiates the necessary signals for reverse doppler operation. The LOAD MEMORY and LOAD MEMORY ERROR signals when detected are respectively stored in FF7 and FF8. Both of these flip-flops are reset when the load memory operation is completed.

The RETURN TO STANDBY (RTS) control message normally resets the transponder station to the standby mode. If RTS is due to a signal drop-out, the transponder station is ready to respond to the reacquisition operation. If RTS is due to maximum range, the transponder station remains in the standby mode until it is

shut off by the 5-minute timer logic. However, the test model transponder station operates in a first-come-first-serve basis. The RTS signal is always treated as if due to a drop-out until further clarification is received from the vehicle. If the previously selected site ID reappears within 3 major frames after RTS, the station control logic simply locks to the reacquired site ID and proceeds on to its normal operating routine. If reacquisition is not accomplished in 3 major frames, the 16-frame counter generates a DELAY RTS signal to erase the station priority. The transponder station is forced to the standby mode. All ON flip-flops are reset to respond to any site ID's associated with the test model transponder station. The DELAY RTS logic is given in the Input Data Register Module, drawing number 69-24436G.

The ON or TRACK control messages from the vehicle are repeatedly transmitted to the transponder station. If either control message and/or its associated site ID are received with parity error, the station control logic ignores the pertinent operation until all data are correctly received. On the other hand the RETURN TO STANDBY control message is transmitted only once. If the transponder station fails to decode RTS for any reason, it also fails to respond to any and all subsequent new site ID's. The 16-Frame Counter, FF2, FF3, FF4, and FF5 of 69-24420G, and its associated logic gates are used to solve this exact problem. Assume that RTS is transmitted by the vehicle and is not properly received by the transponder station. If RTS is due to a drop-out, the vehicle retains the old site ID and transmits an ON control message at the very next major cycle. The station control logic decodes and recognizes the old site ID and its ON control message as if nothing has happened, while keeps on transmitting the old site ID and whatever station status data may be available at the time via the S-band link. However, whether or not the vehicle S-band receiver can reacquire the transponder station signal depends upon the T-state at which the drop-out occurs. If it occurs prior to T-DRC, the vehicle S-band receiver can probably reacquire the transponder station signal

without difficulty. In case that the vehicle fails to reacquire the transponder station in 4 seconds, it transmits another RTS control message. At which time the vehicle either replaces the old site ID with a new one or retains the old one for additional 4-second intervals of reacquisition time. The vehicle makes its decision according to the following rules:

1. If the pertinent site ID is the oldest, it is released and replaced by a new site ID from the vehicle memory.
2. If the pertinent site ID is the newest, it is released and replaced by its alternate site ID.
3. If neither one of the above rules applies, the pertinent site ID is retained and given additional reacquisition time, at 4 second intervals.

If RTS is due to maximum range, the subsequent verifications of the new site ID and the previously selected ON flip-flop do not match. As a result no ON PULSE is generated to reset the 16-frame counter, which counts major frames; i.e., PRESET pulses. At a count of 16 (0000), approximately 2.56 seconds, G26 of 69-24420G generates a signal at P5 time to force the transponder station to the standby mode, which leaves the transponder station with approximately 1.5 seconds to respond to the new site ID. Under normal circumstance 1.5 seconds are more than adequate for the vehicle to verify the new site ID. If the new site ID is not verified within this time interval, the vehicle simply replaces the new site ID by its alternate and starts another 4-second cycle.

5-Minute Timer Module and ID Switches

The 5-Minute Timer consists of an 11-stage ripple counter, FF1 through FF11 of 69-24473G. Its main function is to turn the transponder station pertinent power supplies ON/OFF. Assume both Vcc and VHF sub-bit sync are always available to the station control logic. If the transponder station is in the off mode, the 5-Minute Timer is inoperative. If the transponder station has full power on, D3 provides the necessary signal to turn the

pertinent power supplies off approximately 5 minutes after the detection of the last word sync (111000). The 5-Minute Timer counts S-band frame, T_2CL_{SB} , and is reset by word sync.

When the transponder station is in the off mode, the code control power is off, thus no S-band clock, CL_{SB} , is available to advance the 5-Minute Timer. Therefore, the transponder station remains in the off mode until VHF word sync is detected. The sync pulse resets the 5-Minute Timer and at the same time sets FF12 to turn on the pertinent power supplies. After a nominal turn-on delay, the code control supplies S-band clock pulses to the station control logic. The combination of T_2 and CL_{SB} , which occurs once per S-band data frame or approximately 0.20 sec., is used to advance the 5-Minute Timer, while the sync pulse resets it. As a result, the 5-Minute Timer oscillates between 1 and 0 until the transponder station loses its VHF signal. In the absence of sync pulses the 5-Minute Timer counts T_2CL_{SB} . When it reaches a count of 1536, or approximately 6 minutes, the combined output of G3, G4, and G5 resets FF12. The transponder station is reverted back to the off mode.

The site ID switch bank is used to select the particular station site ID amongst the received VHF data. Only four switches are used in the test model to select the high order four bits of the ID code. The low order two bits are permanently wired. If the four high order bits of the received site ID data match the setting of the ID switches, the ID ENABLE output of G6, which is referred to as the XXXX portion of the ID code, is combined with the two low order bits to strobe the site ID FF. The other logic elements, D1, D2 and G8 are used as inverters and/or to increase the drive capability.

Station Control Encoder Module

The Encoder Module, 69-24444G, is used to generate the required S-band timing and format and encodes the data for S-band transmission. G16 accepts and combines the L_{59} and L_{127} pulses to form $L_{59} + L_{127}$, which is labeled as $2CL_{SB}$. The output of G15,

$L_{59} + L_{127}$, drives a flip-flop, FF4 of the Control Message Detector Module (69-24428G), which divides $L_{59} + L_{127}$ by 2 to provide CL_{SB} and $\overline{CL_{SB}}$.

The S-band data format is described in Section 6.4.1. The 10-bit format is generated by a divide by 10 counter, FF4, FF5, FF6, and FF7 of the Encoder Module. Flip-flops FF4, FF5, and FF6 are connected as a shift register with feedback, G13 and G14. The 10 states of the counter and the corresponding T-pulses are given in Table 6-6. Not all 10 states are explicitly used. Gates G21, G22 and G23 pick out respectively the S-band T2, T3, and T9 (no relation to the Vehicle T-pulses). The S-band timing diagram is given in Figure 6-25.

TABLE 6-6. States of 10's Counter

| T-Pulse | FF4 | FF5 | FF6 | FF7 |
|---------|-----|-----|-----|-----|
| T1 | 1 | 0 | 0 | 0 |
| T2 | 1 | 1 | 0 | 0 |
| T3 | 1 | 1 | 1 | 0 |
| T4 | 0 | 1 | 1 | 0 |
| T5 | 0 | 0 | 1 | 0 |
| T6 | 1 | 0 | 0 | 1 |
| T7 | 1 | 1 | 0 | 1 |
| T8 | 1 | 1 | 1 | 1 |
| T9 | 0 | 1 | 1 | 1 |
| T10 | 0 | 0 | 1 | 1 |

The word sync pattern (111000) is generated by selecting the second half of T2 with G12 and combining it with T3 at G11. G10 is used as an inverter to provide the proper phase for G20. If the TRANSMIT ENABLE signal is low, FF2 is set by T3 through G4 and G5. The ZERO output of FF2 enables the site ID data to pass through either G18 or G19. FF2 is reset at T9, which also sets FF1 for one T-pulse period. The ZERO output of FF1 enables

DATA FORMAT

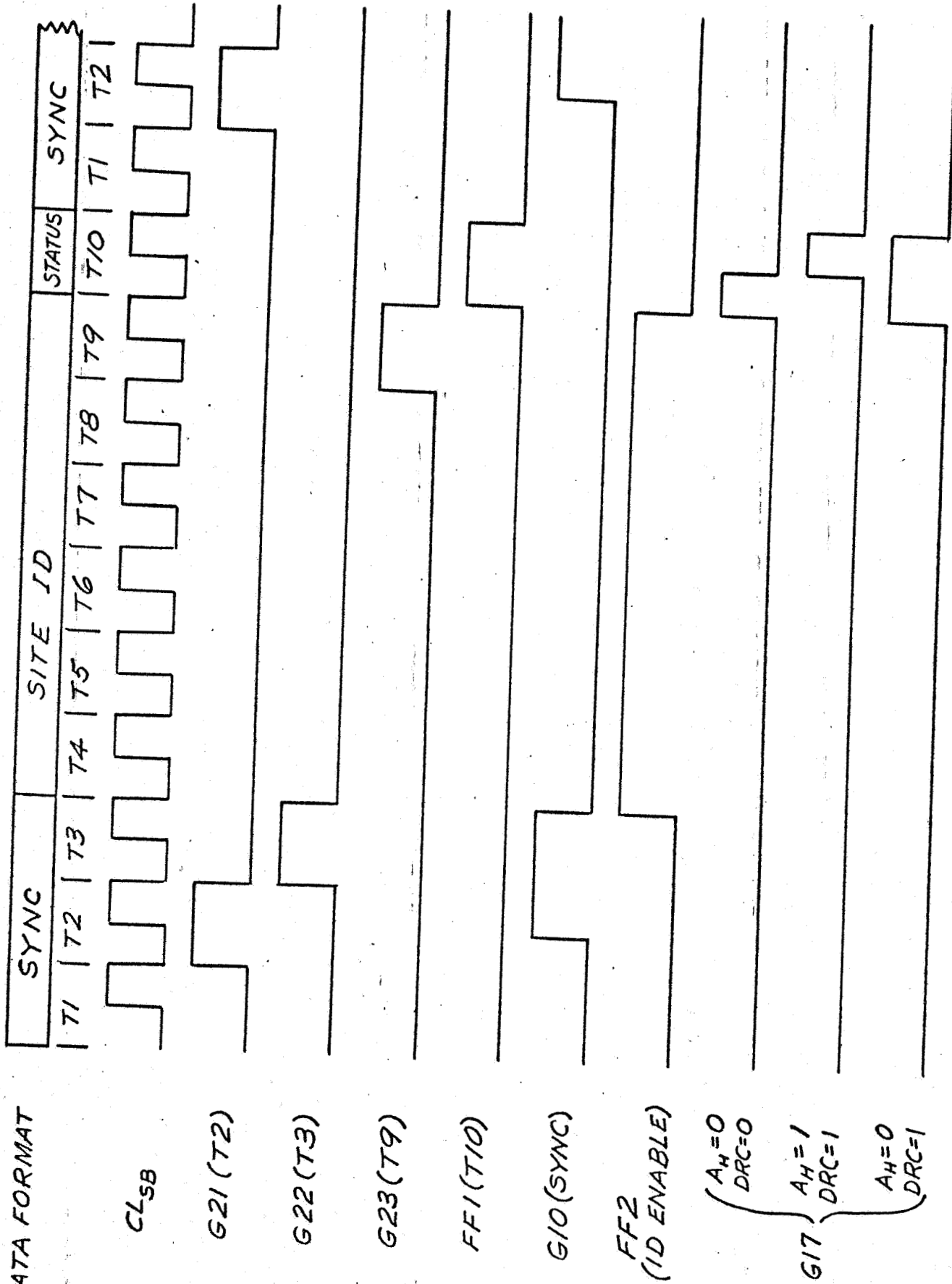


Figure 6-25. S-Band Timing Diagram

the station status data to pass through G17. The significance of the station status bit is given in Table 6-6. The first sub-bit of T10 represents the status of T-A_H and the second sub-bit represents the complement of T-DRC. The sync, site ID data, and station status are combined by G10 to form a single output. The EX/OR, A1, is used as a data selection gate to accept either the output of G10 or external data, such as a new memory program. The actual data selection is determined by the state of FF3. If FF3 is a ZERO, the output of G10 is transmitted to the vehicle, otherwise external data is transmitted to the vehicle. Whenever the LOAD MEMORY SIGNAL becomes a ONE, FF3 is set by T10CL_{SB} to select the external input data and to enable D1 to supply CL_{SB} to the external data source. As long as the LOAD MEMORY SIGNAL remains a ONE, only external data are transmitted to the vehicle. However, this operation is allowed only when the transponder station is in state T-3.

The S-band data format is always generated by the Encoder Module as long as CL_{SB} is available. Whether or not this format is transmitted depends upon the T-state of the transponder station. If the S-BAND ID ENABLE signal is a ONE; i.e., no site ID has been recognized, the output of A1 consists of the sync word pattern (111000) and the station status. The 6 site ID data spaces are filled in with uncoded ONES. However, these data are never transmitted to the vehicle due to the fact that the transponder station site ID and frequency have not been determined. When the station control logic is ready to send the site ID data into the channel, the TRANSMIT ENABLE signal becomes a ZERO so that FF2 can be set or reset by the prescribed T-pulses. As the site ID data come from the ID data register, G18 or G19 encodes each data bit into two sub-bits and inserts them into the S-band data format. The complete format is repeatedly transmitted to the vehicle.

6.4.3 Test Results

Three Station Control Logic Subsystems were built and tested. The test procedure and completed test data sheets are included in (Document No. 12-24472G).

A tester was constructed to operate the Station Control Logic on the bench. The tester was designed to simulate the VHF data from the vehicle and the inputs from the Transponder Code Control unit. The test procedure was written to simulate the actual acquisition procedure as closely as possible. Care was taken to simulate the various possible drop-out modes and to exercise the Station Control Logic in every possible operating mode.

The Station Control Logic subsystems were tested at environmental temperatures of -25°C , $+25^{\circ}\text{C}$, and $+85^{\circ}\text{C}$ and performed very satisfactorily over this range. All outputs were well within specifications. The power supply and inputs were varied over the full dynamic range without degrading in operation.

No design problems were encountered and no particular design improvement is needed.

6.5 STATION TRACKING RECEIVER (1A2)

The station tracking receiver is comprised of five basic functional blocks. They are as follows: Receiver, Code Control, Doppler Inverter, Transmitter Synthesizer, and Transmitter Multiplier/Modulator. Each function is described in the following paragraphs. A simple block diagram showing the relationship of these units is shown in Figure 6-26. For a complete block and interconnection diagram reference to:

Document No. 69-22612H - STATION TRACKING RECEIVER
INTERCONNECTING DIAGRAM.

The overall function of the Tracking Receiver is to acquire and track the downlink signal and to transmit an uplink signal coherent to the received signal which preserves the range and velocity information. It also provides information as to its site ID and its state of operation at any time. The states that the receiver are programmed through are given in Table 6-7.

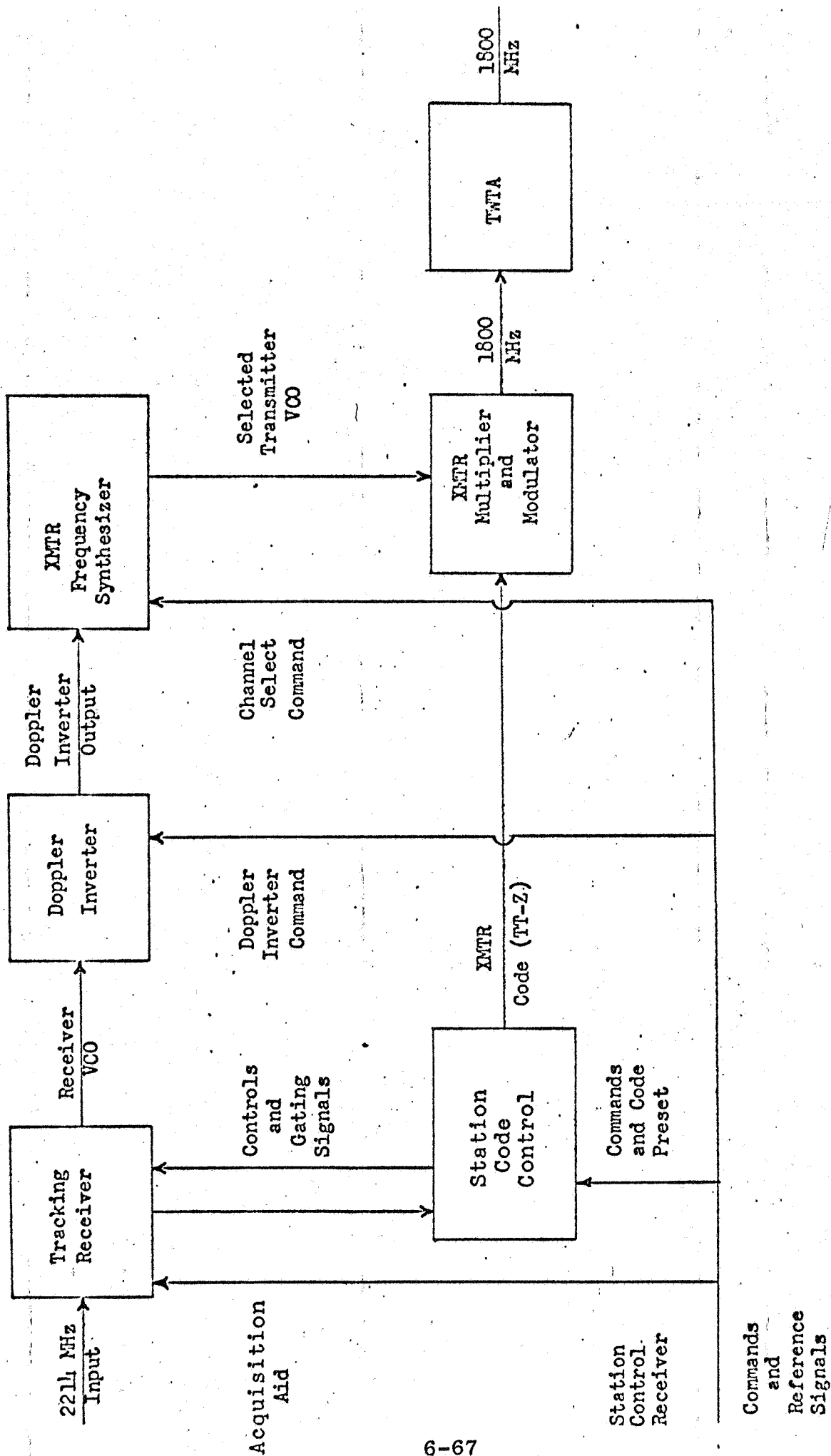


Figure 6-26. S-Band Tracking Receiver Functional Block Diagram

TABLE 6-7. Transponder Station States

| State | |
|-------|--|
| T-0 | L-code preset |
| T-1a | L-code acquired, H-search, reverse Doppler |
| T-2 | Receiver in TRACK, Transmitter code -L code only, reverse Doppler |
| T-3 | Receiver in TRACK, Transmitter code -Full Track code, true Doppler |
| T-1b | L-code acquired, H-search, true Doppler (dropout condition from State T-3) |

In State T-0, the transponder tracking receiver L-code generator is preset to a time uncertainty of approximately one fourth an L-code bit by the VHF link. This eliminates the L-code search. The L-code is acquired and the transponder goes to State T-1a. No waveforms are changed, H-code is automatically acquired, and the transponder goes to State T-2. Transponder State T-2 and T-3 differ only in the retransmitted code. For State T-2 only the L-code is transmitted and for State T-3, the full track code is transmitted.

In the event of signal loss when the receiver is in State T-3, the receiver reverts to State T-1b to try to reacquire the signal.

Station Acquisition is started when the station first receives the VHF control signal from the vehicle. This signal directs the S-band antenna, the VHF carrier frequency presets the S-band carrier, and the VHF modulation presets the S-band L-code. It is possible to adequately define space, frequency, and time so that when the antenna is properly directed, the S-band signal lies within the tracking carrier loop bandwidth and the timing is close enough to define the correct L bit of the incoming code. Hence, by using the VHF signal, the station acquisition is achieved rapidly.

When a vehicle receiver channel becomes vacant, the Vehicle System Control Logic selects a station and transmits the ON instruction. Normally, the transponder is fully acquired in transponder State T-2 and immediately responds with an L-code transmission with reverse Doppler inserted on the carrier. The station transmits the site identification on the S-band data link. The vehicle conducts the L-code search and acquires L-code. At this time the vehicle system control logic verifies the station identification and transmits the TRACK instruction. The transponder sweeps the transmitter carrier from the reverse Doppler condition to the correct Doppler frequency. The vehicle carrier VCO follows the frequency sweep. At the completion of this sweep, the transponder goes from State T-2 to the TRACK mode, State T-3, and notifies the vehicle of this change over the S-band data link.

When the Vehicle System Control Logic decides to drop the station, a RETURN TO STANDBY instruction is transmitted to return the station to the STANDBY mode. The station Tracking Receiver goes to state T-0 and the transmitter is turned OFF. If the station is still within range, the receiver will reacquire and progress to State T-2. A timer in the Transponder Station will return the station to the OFF mode as soon as the Station is out of the range of the VHF signal.

The preceding acquisition sequence has assumed normal operating conditions. Since the AROD system is completely automatic, some provision must be made to alter this sequence during adverse signal conditions. The Vehicle System Control Logic selects a transponder, transmits the ON instruction and channel selection to the transponder. The transponder responds only if the Transponder Tracking Receiver has achieved L-code lock. If the Station ID is not verified in the Vehicle within approximately 4 seconds, System Control instructs the station to RETURN TO STANDBY and selects the next station if the station is the oldest station. The alternate station is called if the station is the

newest station. Otherwise, the station is called until it eventually becomes the oldest station.

If the preceding step is successful, System Control Logic instructs the Transponder to go to the TRACK mode. The station will remove REVERSE DOPPLER and signal the Vehicle that Doppler reverse is complete. The Transponder will then transmit the full track code.

When the S-band signal is first received, the L-code locks and A_L goes to a ONE. The code control unit goes to Step T-1(a). The station control logic will then accept the ON instruction.

After A_L goes to a ONE, if A_L goes to ZERO for >0.1 second, the code control unit returns to Step T-0. The S-band transmissions are turned off.

When A_H goes to ONE, the code control unit goes to State T-2. If A_H goes to ZERO for >0.1 second, the code control unit starts a timer. After 2.5 seconds the code control goes to state T-0 to reacquire. The S-band transmissions are turned off in state T-0.

In the ON mode, the transponder will accept a TRACK instruction. Upon receipt of the TRACK instruction, the Station Control Logic signals and the Station Frequency Synthesizer to remove reverse Doppler and upon completion of this instruction, the Station Frequency Synthesizer notifies Station Control. Station Control then signals the code control unit to go to State T-3.

- a. If A_H goes to ZERO FOR >0.1 second, the code control unit goes to State T-1b. After 2.5 seconds the code control goes to Step T-0 to reacquire.
- b. If the Station is instructed to go from the TRACK mode to the STANDBY mode, i.e., the vehicle lost lock and desires to reacquire, the transponder code control reverts to State T-0, REVERSE DOPPLER is inserted and the acquisition sequence proceeds from that point.

6.5.1 S-Band Receiver

The receiver, consisting of two distinct phase locked loops, is contained in 11 modules: 1A2A1 through 1A2A9, 1A2A21 and 1A2A22. See reference 6 for detail design and description information. The carrier and modulation are tracked in separate loops on a time shared basis. A functional block diagram of the receiver is shown in Figure 6-27. The basic signal relations may be observed from Figure 6-28.

Let $m_1(t)$ represent the transmitted signal modulation. Consider for simplicity the case when the Vehicle Tracking Receiver is receiving the L code only. Then $m_1(t)$ is the transmitted L-code. For simplicity, this appears as balanced amplitude modulation which is identical to bilevel, ± 90 degree phase modulation.

Then at (1) in Figure 6-28 the signal is $m_0(t + \tau)m_1(t) \sin(\omega_1 t + \theta_1)$. $\theta_1 - \theta_0$ is the tracking error in the ranging loop. $m_0(t + \tau)$ can be represented by $m_1(t + \tau) F_L(t + \tau)$ where $F_L(t)$ is a square wave whose fundamental frequency is F_L . If τ is zero then $m_0(t) M_1(t)$ clearly equals $F_L(t)$. The spectrum at (1) is then as shown in Figure 6-14.

Figure 6-29 represents the case when the range tracking error is real but small compared to one bit length. Not shown, but present, is a small amount of "wideband noise" due to the uncorrelated parts of m_0 and m_1 . When $|\tau| > 2T_L$ only this "noise" appears. It has a bandwidth equal to more than $2F_L$ and is relatively uniform across the bandwidth. Notice that when $\tau = 0$ there is no signal at f_1 . When τ has some magnitude, but small compared to $2T_L$, both the carrier component at f_1 and the even harmonics of the square wave begin to appear. The magnitude of the component at f_1 is proportional to $\frac{|\tau|}{2T_L}$. The phase of this component is zero degrees relative to θ_1 when $\tau > 0$ and is $\theta_1 + \pi$ when $\tau < 0$.

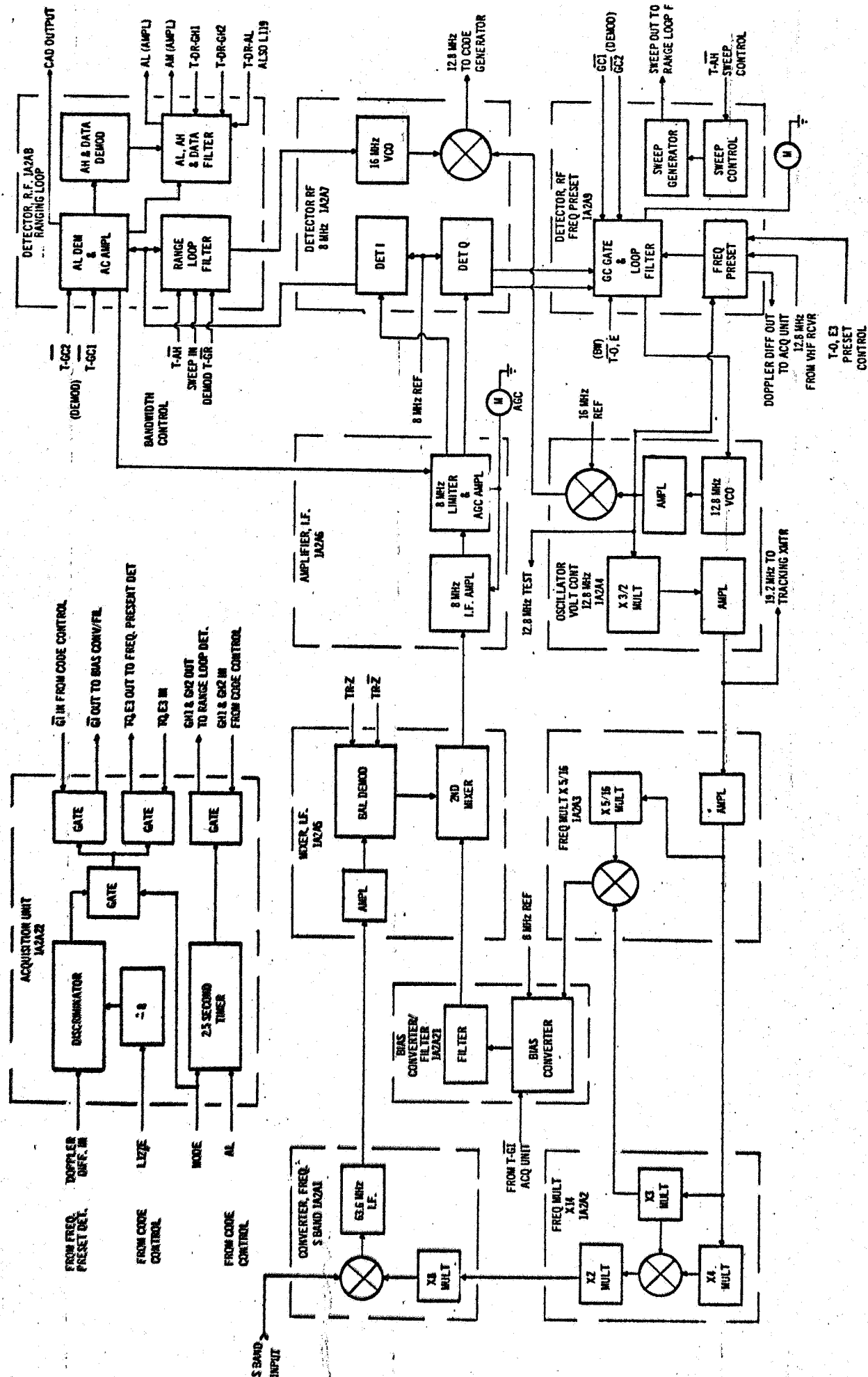


Figure 6-27. S-Band Receiver

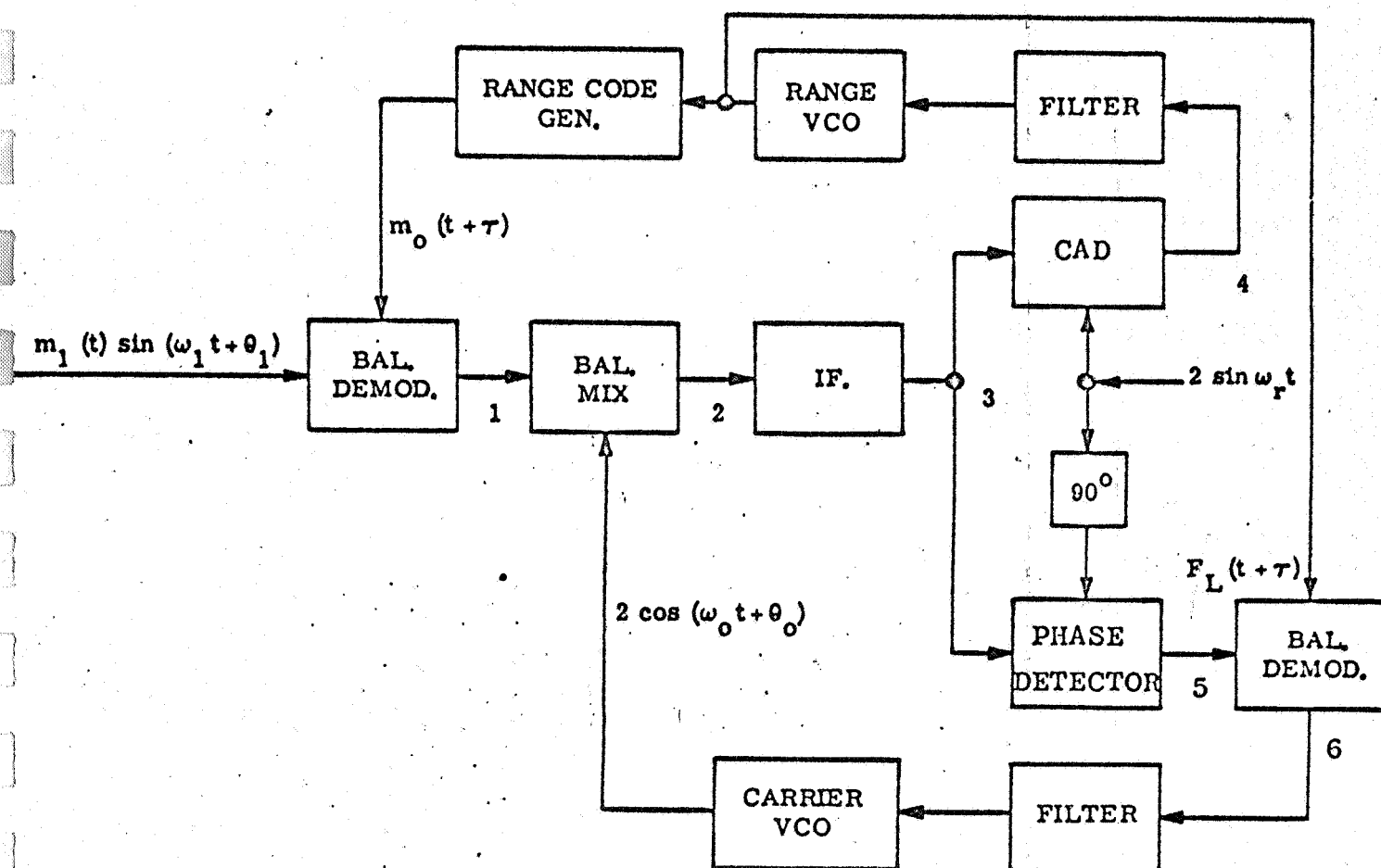


Figure 6-28. S-Band Signal Processor, Functional Block Diagram

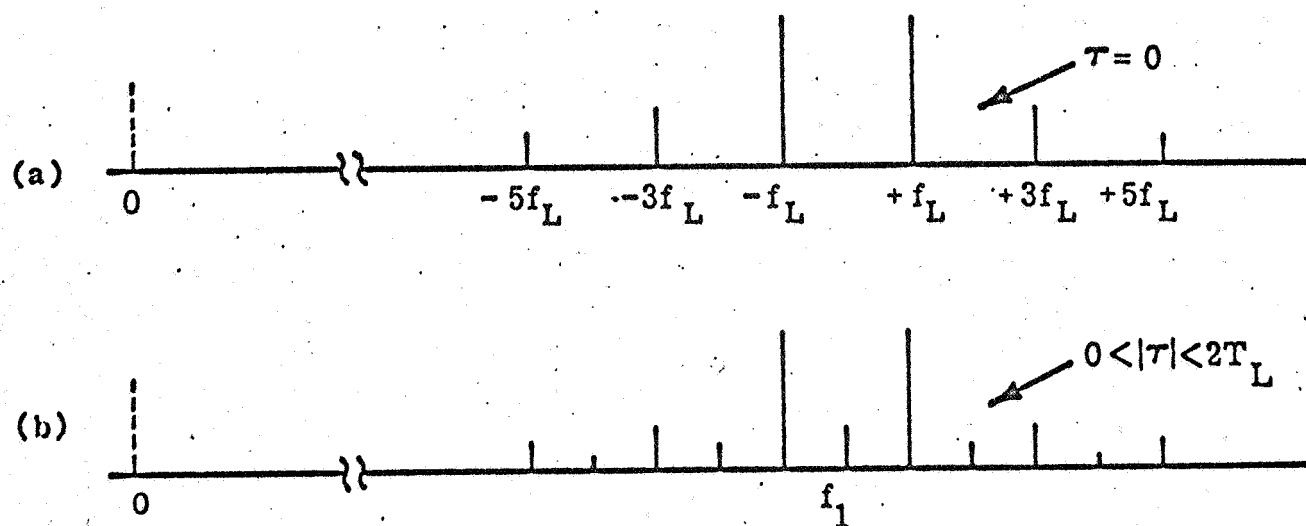


Figure 6-29. Spectrum of Signal at Pt. (1)

At (2) the signal is $m_o(t + \tau) m_1(t) \sin [(\omega_1 - \omega_o)t + a_1 - a_o]$. This signal appears exactly as at point (1), except that it is shifted down in frequency from f_1 to $f_1 - f_o$. The phase of the "carrier" component is now $a_1 - a_o$ or $a_1 - a_o + \pi$ depending upon the sign of τ .

If the bandwidth of the intermediate frequency is wide compared to F_L , then the signal at (3) is essentially identical to that at (2). If $f_1 - f_o$ is equal to f_r then at (4) the signal is $m_o(t + \tau) m_1(t) \cos (a_1 - a_o)$.

The spectrum of the signal at (4) appear as shown in Figure 6-30.

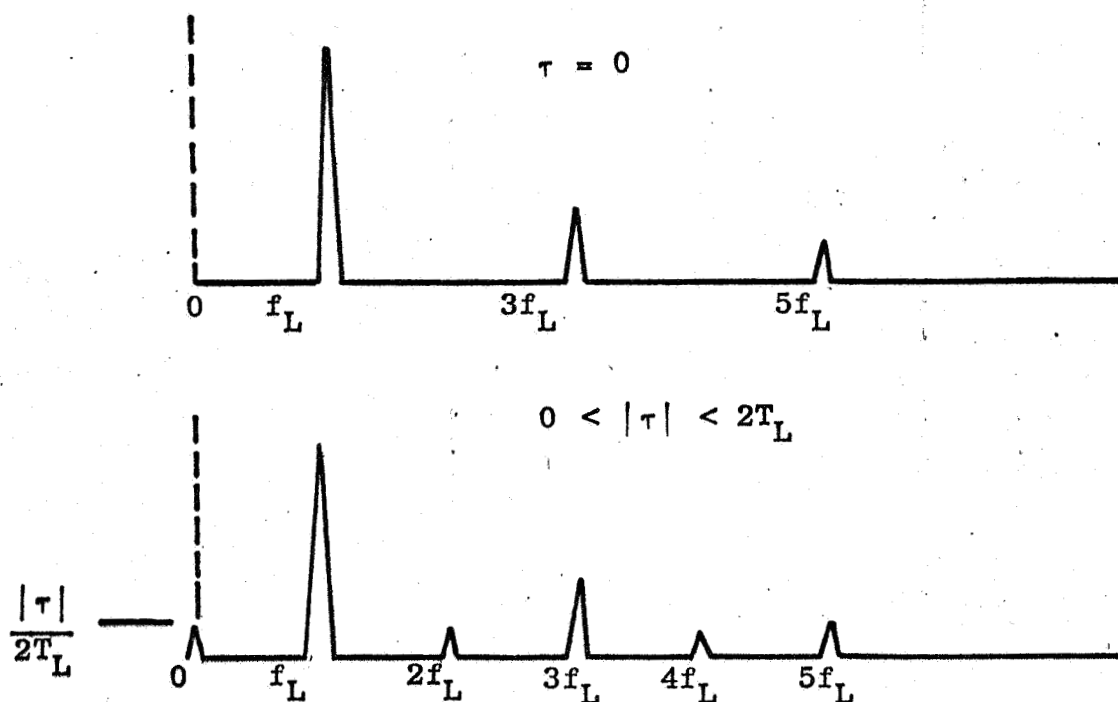


Figure 6-30. Spectrum of Signal at (4) for Small Error τ

The range tracking error signal at dc is proportional to $\frac{\tau}{2T_L}$, $|\tau| < \frac{T_L}{2}$ modified by the cosine of the carrier tracking error. But the error in the carrier loop is constrained to be small and, therefore, it only has a second order effect on the gain of the range tracking loop. This D-C error signal is used to control the range tracking VCO to drive τ to zero. Thus the range tracking control signal is carried by the presence of a carrier component at f_1 at point (1) and it is sign sensitive to the sign of τ .

The signal at (5) is $m_o(t + \tau) m_1(t) \sin(a_1 - a_o)$. If $a_1 - a_o = 0$ then there is no signal at (5). For small error, $a_1 - a_o$, the signal is essentially an error, $\epsilon = a_1 - a_o$, whose magnitude is $m_o(t + \tau) m_1(t)$. The balanced demodulator between (5) and (6) multiplies the signal at (5) by $F_L(t + \tau)$. Therefore, since $m_o(t + \tau) = m_1(t + \tau) F_L(t + \tau)$ the signal at (6) is $m_1(t) m_1(t + \tau) \sin \epsilon$ since $F_L(t + \tau) F_L(t + \tau) = 1$ everywhere. For small τ , $m_1(t) m_1(t + \tau) = 1$ so that the d-c signal is proportional to $\sin(a_1 - a_o)$, the typical phase-locked loop error signal.

In this case the carrier tracking signal is carried by the sidebands of the signal at (1). Thus the two loops have interchanged the normal role of error signals. The modulation error signal is proportional to the magnitude and sign of the carrier component at (1) and the carrier tracking signal is proportional to the phase of the sidebands of the signal at (1).

A little reflection will show that this process largely removes tracking errors caused by phase and amplitude variations of the narrowband filters, the gain control circuits, and the majority of the receiver amplification. These appear only as gain variations in the control loops and eliminate the largest contributor of tracking error which confronts most range tracking systems.

Functional Description

The Frequency conversion and I-F Amplification Module 1A2A1 contains the S-Band Converter X8 LO multiplier, and wideband First I-F. The module has a nominal gain of 20 dB, input noise figure of 8 dB and bandwidth of ± 15 MHz. The I-F signal is delivered to module 1A2A5 which contains the wideband Balanced Demodulator and the second mixer. The 8 MHz output is then fed to 1A2A6 which contains the 8 MHz I-F and limiter and AGC Amplifier. The module has a gain range of +10 to +80 dB. The signal is then applied to 1A2A9 which contains a phase detector for carrier tracking (Detector Q) and to a coherent amplitude detector (Detector I) from which the following signals are derived.

1. AGC
2. L-code acquisition sensing signal, A_L
3. H-code acquisition sensing signal A_H
4. Range error signal.

During step T-0, L-code preset, a noncoherent AGC detector is used to stabilize the signal levels into the threshold detectors. This action also limits the bandwidth expansion of the carrier loop under strong signal conditions.

Once the L-code in the receiver is properly aligned, the signal to the balanced detectors is a sine wave balanced modulated by a square wave whose fundamental frequency is F_L . Therefore, the output of the balanced detector I is a square wave whose amplitude is proportional to the cosine of the carrier error. This signal is demodulated by a balanced modulator which is represented by the gating signal G_c . Coherent AGC voltage is now present at this point and the noncoherent AGC voltage is removed.

The output of the balanced detector Q is also a square wave whose fundamental frequency is F_L , but the amplitude is proportional to the sine of the carrier error. This signal is amplified in a video amplifier and demodulated by a full wave demodulator which is represented by the G_c gates. The carrier error control signal is a D-C signal and proportional to the sine of the carrier phase error.

This method of demodulation for carrier control allows the phase detector to be A-C coupled and therefore the signal can be low level, well below the normal D-C bias point of conventional phase detectors.

The recovery of demodulation of the other signals is performed in the in-phase phase detector (Phase Detector I) and the subsequent detectors.

The presence or absence of the coherent AGC signal in Steps T-0 and T-1A constitutes the L-code acquisition signal, A_L . The Detector I output is amplified in a power video amplifier and demodulated for AGC, and A_L , in a balanced demodulator which is exactly the same as the balanced demodulator of the carrier control loop. In steps T-1A and T-2, AGC and A_L are demodulated during the same intervals as the carrier control. The H-code acquisition signal, A_H , is derived in the same manner as the AGC signal. However, it is available only in step T-1A and step T-2. The appearance of A_H automatically switches the receiver system from step T-1A to step T-2. In step T-1A a reference signal is generated which can result in a proper A_H during all H-code intervals.

AGC, A_L , A_H are all balanced, modulated A-C signals at the Detector I input. A-C coupling to the balanced detectors is therefore satisfactory. The same is true for carrier control.

Range error control is more difficult and warrants further explanation. During steps T-0 and T-1A the same F_L square wave appears at the range demodulator input. If the L-code is exactly aligned, the input signal appears as an idealized square wave.

However, if there is some misalignment, the square wave becomes unsymmetrical. The ranging loop is gated open for an interval equal to $T_L/2$ seconds and bracketing the positive going zero crossings of the F_L square wave. The uncorrelated portion of the signal averages to zero. The range error control signal, the correlated portion of the received signal, has an average which is nonzero. This average is positive or negative depending upon the lead or lag of the receiver reference L-code.

A-C coupling, of course, causes the long term average to be zero in any event. However, the action of the gate is to average the result only during the period when the gate is open. This is equal to the long term average only when there is no error. The average during the gated interval differs from the long term average as a function of the tracking error and is sign sensitive.

In step T-2 the ranging is performed only during those intervals when the reference is $L \oplus H \oplus F_H$ or the second and third quarters of the even numbered L-code bit intervals. Once again the control signal is the difference between the tagged average and the over-all average.

Local Oscillator Synthesis

The first and second LO multiplication is accomplished in two modules, 1A2A2 and 1A2A3. Since the S-band signal may range from 2200 to 2450 MHz, the LO frequencies will change. The proper multiplier ratios may be determined for any frequency with the aid of Figure 6-31. For the carrier loop to be locked, the signals at the phase detector must be the same frequency.

$$\text{i.e., } f_{in} - 8LMf_v - LNf_v + f_r = f_r$$

after rearranging and canceling terms

$$f_{in} = 8LMf_v = LNf_v$$

or

$$L(8M + N) = \frac{f_{in}}{f_v}$$

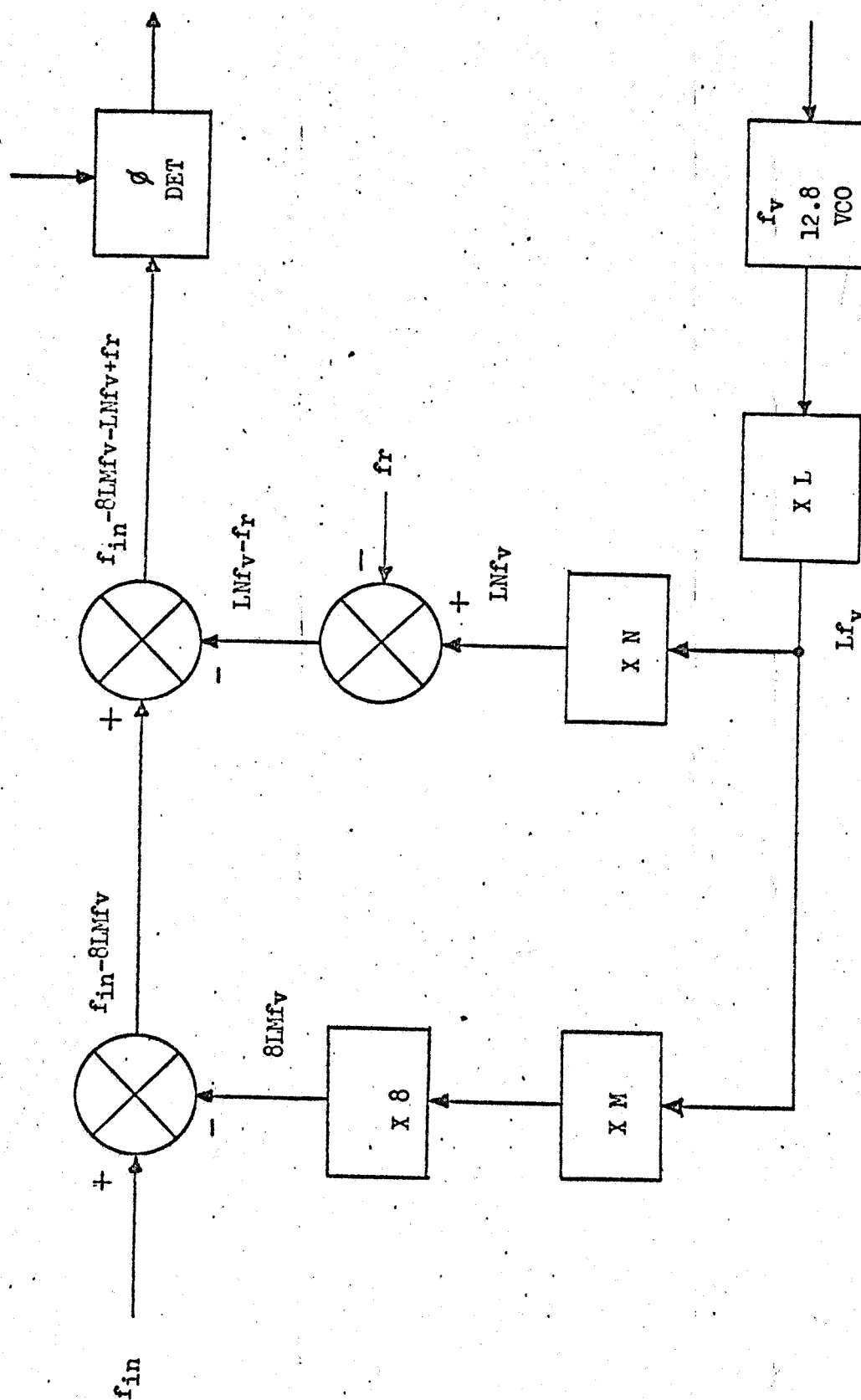


Figure 6-31. Local Oscillator Multiplier Synthesis

Now f_v is fixed at 12.8 MHz and f_{in} is constrained in the following manner: $f_{in} = (2200 + 0.4 k)$ MHz, that is, f_{in} is selectable in 400 kHz increments, $k = 1, 2, \dots, 625$.

Then:

$$L(8M + N) = \frac{22000 + 4k}{128} = 171 + 7/8 + k/32$$

$$L(8M + N) = 171 + \frac{28 + k}{32}$$

We will constrain L to be 1 or $3/2$.

For a signal of 2214 MHz

$$k = \frac{14}{0.4} = 35$$

$$L(8M + N) = 171 + \frac{63}{32} = 172 + \frac{31}{32}$$

Rearrange numbers:

$$\begin{aligned} L(8M + N) &= 8(21 + \frac{1}{2}) + \frac{31}{32} \\ &= 8 \times 21 + 4 + \frac{31}{32} = 8 \times 21 + \frac{159}{32} \end{aligned}$$

$$\text{Let } L = \frac{3}{2}$$

$$\begin{aligned} L(8M + N) &= \frac{3}{2} (8 \times 14) + \frac{3}{2} \left(\frac{53}{16} \right) \\ L(8M + N) &= \frac{3}{2} \left(8 \times 14 + 3 \frac{5}{16} \right) \end{aligned}$$

Then

$$L = 3/2$$

$$M = 14$$

$$N = 3-5/16$$

and the synthesis is complete.

Bias Converter

The Bias Converter/Filter (1A2A21) is added into the 2nd LO Chain to subtract errors associated with the phase detector reference signal. The bias converter also contains a gate which opens the LO Chain and correspondingly the signal path during certain periods in the track mode.

Frequency Preset and Acquisition Unit

Initial Acquisition of the carrier is aided by the frequency preset module. The carrier loop VCO is compared with the VHF carrier loop VCO which is locked to a signal with the proper Doppler. The preset develops a D-C error voltage which is used to preset the Tracking Receiver VCO thus virtually eliminating frequency search. An additional output from the Preset module, the actual frequency difference of the two VCO's, is fed to module 1A2A22 (Acquisition Unit).

Because of the multiplicity of L-code sidebands, the tracking receiver could easily lock to any one of several such sidebands as the VCO is swept by the preset to its proper frequency. The Acquisition Unit acts as an antiseband lock device. It compares the received Doppler difference frequency with a fixed 6 Hz signal. If the Doppler difference is less than the reference, the receiver is allowed to lock. If the difference is greater, the bias converter gate is pulsed to open the loop instantaneously and release the sideband lock. In this manner the receiver steps along until the carrier is captured. When the receiver achieves state T-2 or T-3 the Acquisition Unit is inhibited. This is done to insure that Doppler differences between the two receivers will be ignored in the event that the control receiver loses lock while the Tracking Receiver is in the full Track mode.

The Acquisition Unit performs one other function. Upon acquisition of L-code the receiver is frozen in T-1A for approximately 2.5 seconds to allow damping of transients in the range loop. The high code is then allowed to lock and the loop goes to T-2.

Rate Aid

Rate Aid is incorporated in the receiver to free the ranging loop from the tracking Doppler offsets. Figure 6-32A shows this implementation.

f_r = Range loop VCO frequency (16 MHz)

f_{re} = Range loop error

f_o = Reference frequency (16 MHz)

f_{oe} = Reference frequency drift 1×10^{-7} part/month

f_c = Carrier loop VCO frequency

f_D = Doppler shift from f_c

The resultant rate aid is 100 percent within 1×10^{-7} parts/month which is the stability of the station clock.

Test/Operate Switch

A switch on the rear panel of the Tracking Receiver Drawer is used to interrupt the T-0 signal from the code control logic to the station control logic during testing. In normal operation the T-0 signal is used to inhibit any decoded ON instructions that the control logic receives. Therefore the tracking receiver cannot transmit while it is in T-0.

In the test mode the line is opened and the control logic side is grounded. This allows ON instructions to be relayed to the Tracking Receiver.

This is necessary since the Tracking Transmitter is translated in frequency and used as the input signal to the tracking receiver.

Since the receiver cannot move from T-0 until it receives a signal to which it can lock, and the transmitter cannot be turned on until the receiver is locked, the Station Control Logic inhibit function must be removed during test.

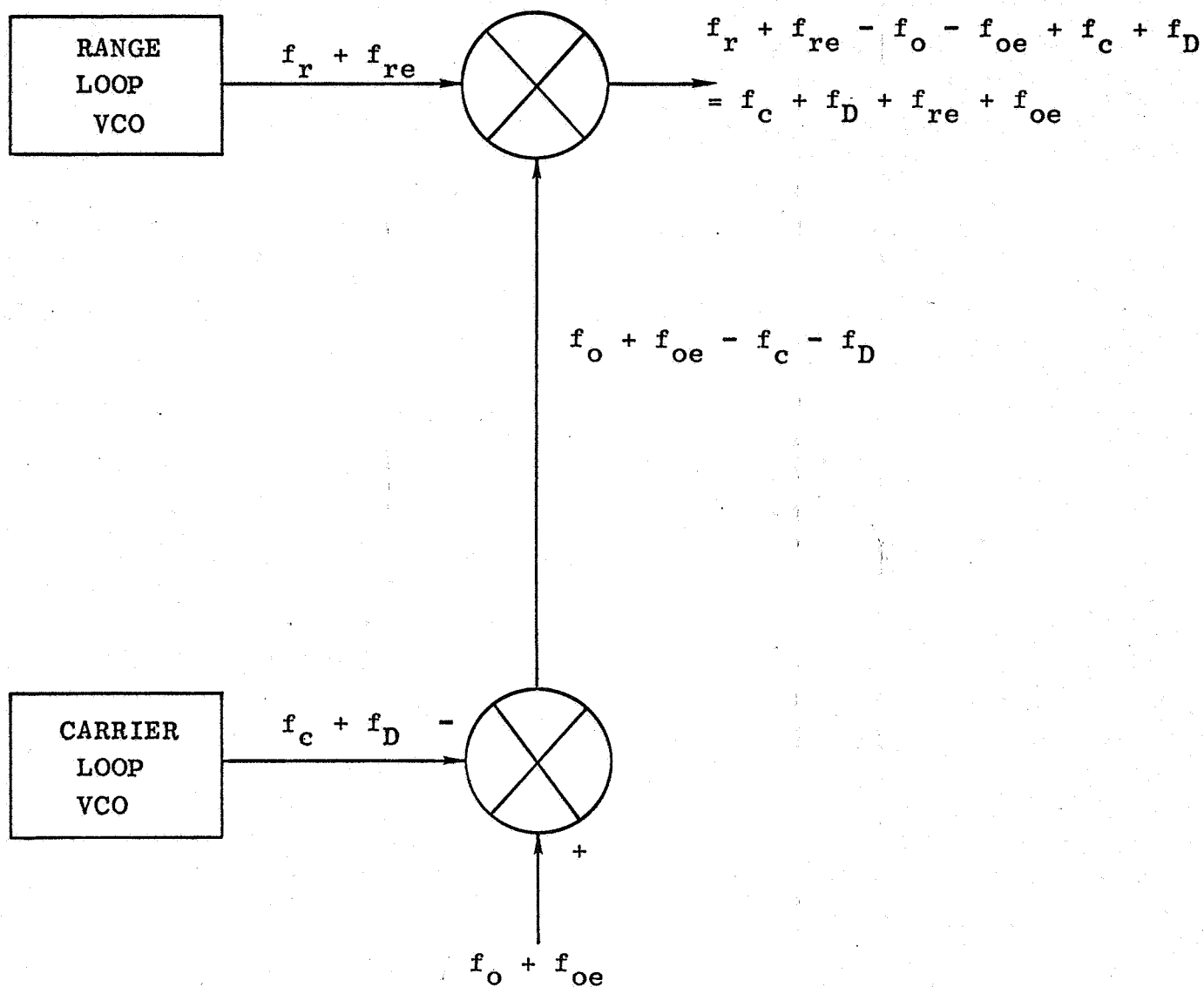


Figure 6-32A. Rate Aid Loop

6.5.2 Code Control

The Code Control generates two PN codes; one code is used to demodulate the ranging code received from the airborne stations, the other is the ranging code that is transmitted to the airborne station. It also supplies accurate timing and state signals to other subsystems.

In order to achieve the high phase stability required for the two PN codes and timing signals, it was necessary to use a maximum clock frequency of 12.8 MHz. Special hybrid high speed flip-flop output circuits were used to minimize phase shift and insure fast rise and fall times for the PN codes.

Since the forms of the demodulation signals and transmitted code signals depend on the relative phase (or degree of correlation) between the received code and the local reference, a programmer is required whose state will depend on the relative phase of these two signals. It must be possible to acquire the received code rapidly, and to include data bits in the transmitted code. In addition, the variation in phase difference between received and transmitted ranging modulation must be kept very small.

The high speed component, the H-sequence, has a bit rate of 6.4 MHz and a period of 511. The low speed component, the L-sequence, has a bit rate of 6.4/1022 MHz and a period of 127. Both sequence generators are capable of being preset by an external signal. Gating signals for use by the receiver are generated by timing signals derived from the two sequence generators. The transmitter code includes provision for combining a data bit stream with the coded modulation. The acquisition procedure and form of the transmitter and receiver codes and gating signals are dependent upon which state of the acquisition procedure is in process. The states are denoted by T-0, T-1A, T-2, T-3, and T-1B. This program sequence is shown in figure 6-32B, while the forms of these signals are given in Table 6-8. All timing signals are derived from the 12.8 MHz input frequency, whose analog form is denoted by $T-2f_H$ and whose digital form is denoted by $T-2F_H$.

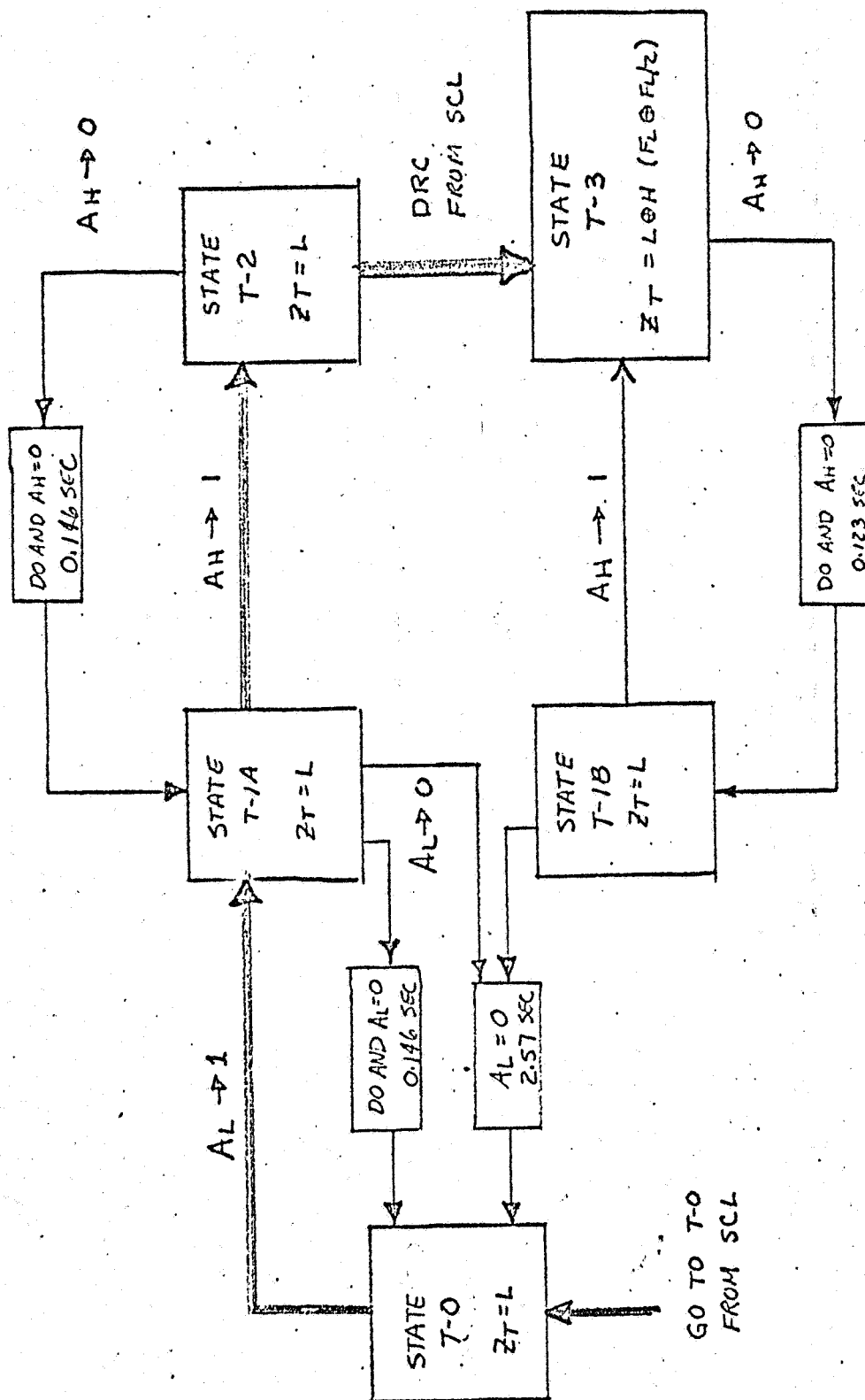


Figure 6-32B. Transponder Code Control States

TABLE 6-8. Logic Equations

$$TT-Z = L \oplus H(F_L \oplus F_{L/2}) (T-3) \oplus D'$$

$$TR-Z = F_L (L_{2N} + 1 + T-0 + T-1A + T-1B) \oplus L \oplus H(F_L \oplus F_{L/2}) \\ \oplus L_{2N} (T-2 + T-3) (F_L F_H + F_{L/2} F_H + F_L F_{L/2})$$

$$GI = (T-0 + T-1A + T-1B) + (F_L \oplus F_{L/2})$$

$$GR = (T-0 + T-1A + T-1B) (\bar{F}_L \oplus F_{L/2}) (P-GR) + (T-2 + T-3) \\ (F_L \oplus F_{L/2}) L_{2N}$$

$$GH1 = (L_{2N} + 1 + T-0 + T-1A + T-1B) \bar{F}_L F_{L/2}$$

$$GH2 = (L_{2N} + 1 + T-0 + T-1A + T-1B) F_L \bar{F}_{L/2}$$

$$GC1 = (T-0 + T-1A + T-1B) \bar{F}_L \bar{F}_{L/2} + (T-2 + T-3) L_{2N} + 1 \bar{F}_L F_{L/2}$$

$$GC2 = (T-0 + T-1A + T-1B) F_L F_{L/2} + (T-2 + T-3) L_{2N} + 1 F_L \bar{F}_{L/2}$$

where: $N = 0, 1, 2, \dots, 58$

Before discussing the logic design in detail, some definitions and conventions will be stated.

1. Buffer elements perform NOR logic so that an enable signal input to a buffer element is considered to enable the element when the signal is at a "zero" level.
2. H_{N-i} and L_{N-j} are the outputs of the i -th stage of the H-sequence generator and the j -th stage of the L-sequence generator, respectively.
3. The bits of the H- and L-sequences are defined by the following recursion formula and initial conditions.

$$a. \quad H_k = H_{k-9} \oplus H_{k-4} \quad k = 10, 11, 12, \dots, 511 \\ H_1 = H_2 = H_3 = H_4 = H_5 = H_6 = H_7 = H_9 = 0 \\ H_8 = 1$$

$$\begin{aligned}
 \text{b. } L_m &= L_{m-7} \oplus L_{m-6} \quad m = 8, 9, 10, \dots, 127 \\
 L_1 &= L_2 = L_3 = L_4 = L_5 = L_7 = 0 \\
 L_6 &= 1
 \end{aligned}$$

Note that when H_k appears as the output of H_{N-9} , H_{k+1} through H_{k+8} are the output of H_{N-8} through H_{N-1} , respectively; and similarly, when L_m appears as the output of L_{N-7} , L_{m+1} through L_{m+6} are the outputs of L_{N-6} through L_{N-1} , respectively. The notation, H_k and L_m , will be used interchangeably to denote the k -th or m -th bit of the H or L sequence, respectively, or to denote signals which are "one" when H_k or L_m appear as outputs of H_{N-9} or L_{N-7} and "zero" at all other times. Thus L_{127} might refer to the 127th bit of the L sequence, or to a signal which is a "one" only when L_{127} is the output of the last stage of the L sequence generator. This usage should cause no confusion since the context in which the notation is used will clearly indicate whether the bit or the signal is referred to.

Code Control Logic Diagrams

| <u>Module</u> | <u>Logic Diagram</u> |
|---------------------------|----------------------|
| Code Clock Generator | 69-23408G |
| GR Gates | 69-26252G |
| H-Sequence Generator | 69-23409G |
| L-Sequence Generator | 69-23410G |
| S-Band Data Encoder | 69-23411G |
| Code Preset | 69-26232G |
| Input Control | 69-23384G |
| Programmer and DO timer | 69-24461G |
| R/A Timer | 69-24465G |
| Buffer Module | 69-23389G |
| Gate Generator | 69-23372G |
| Transmitter Code Combiner | 69-23376G |
| Receiver Code Combiner | 69-23368G |

Clock Signal Generation

All fundamental clock and timing signals are generated by using three modules consisting of the Code Clock Generator, the GR Gates, and the H-Sequence Generator. The input signal $2f_H$ is shaped and buffered to form the signal $\overline{2F_H}$. This signal is further divided by two and buffered to form HCL Enable. $\overline{2F_H}$ is inverted by a buffer element to form $2F_H$ and is combined with HCL Enable to form the 6.4 MHz clock signal denoted by HCL. $\overline{2F_H}$ is also combined with the LCL Enable to form the 6.4/1022 MHz clock signal denoted by LCL. By forming clock signals in this manner, the only timing variations (or clock skew) will be the differential propagation delay through different buffer elements. A 6.4 MHz square wave is reclocked by $2F_H$ to form the F_H signal.

The following list identifies the signals of interest on this drawing.

| <u>Signal Number</u> | <u>Signal Name</u> |
|----------------------|----------------------|
| 2 | $\overline{2F_H}$ |
| 4 | HCL ENABLE |
| 5 | HCL |
| 6 | $2F_H$ |
| 7 | F_H |
| 9 | \overline{H}_{511} |
| 10 | LCL ENABLE |

It should be remembered that only every other H_{511} pulse will generate an LCL Enable interval.

The H-Sequence Generator module contains a standard linear shift register generator of nine stages and three word detectors. The three word detectors are connected so that one has a "one" output during code bit H_{225} , one has a "one" output during code bit H_{510} , and one has a "one" output anytime the first eight

stages contain "zero". This latter word detector is used to insure that the generator will not lock up in the "all-zero" condition. H_{510} and H_{255} are used by the Code Clock Generator to generate F_L , $F_{L/2}$, $F_L \oplus F_{L/2}$, and LCL Enable as described below. This sequence generator includes provision for changing the phase of the sequence. This provision is the H-Shift input. This signal line is normally held at a "zero" level, and when the signal is raised to a "one", a "zero" will be shifted into the second stage. If this signal is made a "one" for one cycle of HCL following H_{510} , the sequence generator will contain the following sequence.

| H Shift | H_{N-1} | H_{N-2} | H_{N-3} | H_{N-4} | H_{N-5} | H_{N-6} | H_{N-7} | H_{N-8} | H_{N-9} | |
|---------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | H_{510} |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | H_{511} |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | H_0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | H_{511} |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | H_1 |

It is seen that two additional states have been added to the sequence in that H_0 has been forced into the register and H_{511} has been repeated. Hence H_1 appears 2 bit times later and the sequence has been delayed by 2 bits. Since the sequence length is odd, any delay from 1 to 510 bits, inclusive, may be accomplished.

H_{510} and H_{255}^* are retimed by HCL in the Code Clock Generator to become H_{511} and H_{256} respectively. The "one" to "zero" transition of F_L will coincide with the "one" to "zero" transition of H_{511} , and the "zero" to "one" transition of F_L will coincide with

*Note that these signals are defined to be a "one" when H_{510} and H_{255} , respectively, appear as outputs of stage H_{N-9} ,⁵¹⁰ and "zero" otherwise.

the "one" to "zero" transition of H_{256} . Transitions of $F_{L/2}$ will coincide with the "one" to "zero" transitions of H_{511} , while transitions of $F_L \oplus F_{L/2}$ will coincide with the "one" to "zero" transitions of H_{256} . Note that H_{256} , H_{511} , F_L , $F_{L/2}$, and $F_L \oplus F_{L/2}$ appear at the output terminals of register elements which are all clocked by the same HCL. H_{511} , $F_{L/2}$, and F_H are combined to form LCL Enable in a manner which will allow LCL to be coincident with the HCL pulse which caused $F_{L/2}$ to make a "one" to "zero" transitions.

L-Sequence Generator

The module consists of a 7-stage shift register generator with synchronous preset capability, three word detectors, and a re-timing circuit. One word detector is to prevent lock up in the "all-zero" state and detects "zeroes" in the first six stages of the register. Another word detector is connected to detect "zeroes" in the first six stages and "one" in the last stage. This stage of the generator occurs during bit time L_{126} . The signal from this detector is retimed and becomes the L_{127} signal. The remaining word detector is set to detect "ones" in the first six stages and "zero" in the last stage which occurs at bit time L_{119} . When the L-Search signal is "zero", this L_{119} signal will force the next state of the register to be L_{121} instead of L_{120} by causing a "zero" to be set in the first stage instead of a "one". Thus, the phase of the L-sequence will change at a rate of one L sequence bit per L-sequence period when the L-Search signal is at a "zero" level. When this signal is at a "one" level, the L-sequence phase shifting circuits are inhibited.

The synchronous preset capabilities are utilized when the EM + L SYNC signal goes to "one" or when both this signal and the L SYNC signal goes to "one". When both signals are held at a "one" level, the 7 bit word 1000000 is continuously set into the first through the seventh stages by LCL until both signals

go to a "zero" level. This condition sets the L-sequence generator, such that the first full L-sequence bit after the EM + L SYNC and L SYNC signals go to a "zero", is 0100000 which is the L_1 bit time. In a similar manner, making only the EM + L SYNC signal a "one" will cause the state 1010110 to be set into the register. The first full L-sequence bit after the EM + L SYNC signal goes to "zero" will then be 1101011 which is the L_{75} bit time.

S-Band Data Encoder

This module contains an L-Sequence Generator word detector for detecting L_{58} , three retiming circuits, and a four stage presetable counter with logic for generating the bit sequence L_{16N+1} , L_{16N+9} , and L_{8k+1} (for $N = 0, 1, \dots, 7$ and $k = 0, 1, \dots, 15$) and the bit stream, D' .

The word detector is connected to the L-Sequence generator module to detect the bit pattern 0011100 which occurs during bit time L_{58} . This detector output is retimed by LCL to yield the signal called L_{59} .

The four stage counter is preset by L_{127} and synchronously divides the LCL rate by 16 so that the L-Sequence period is divided into 7 intervals of 16 L-Sequence bit times each and one interval of 15 L-Sequence bit times.

The three word detectors attached to the counter form the three required bit sequences. The bit sequence L_{8k+1} is retimed by LCL to form the bit sequence L_{8k+2} . The bit sequence L_{16N+1} and L_{16N+9} are combined with the Data input signal according to the following equation to form the steering signal, $S-D'$.

$$S-D' = (DATA) (L_{16N+1}) + (\overline{DATA}) (L_{16N+9})$$

This signal is then retimed by LCL to form the D' signal.

GR Gates

In addition to buffering three timing signals, this module is required to form the interval between H_{385} and H_{151} for use in deriving the GR gating signal. The bit pattern 0110 __ 0000 in stages H_{N-1} through H_{N-9} , respectively, is detected and retimed to become the pattern 00110 __ 000. This is the pattern at bit times H_{151} or H_{384} depending on the output of H_{N-6} . This pattern is then combined with H_{N-6} so that the output flip-flop is set to "one" if H_{N-6} is "zero" and is set to "zero" if H_{N-6} is "one". The flip-flop is clocked by HCL so that its output, P-GR, will become a "one" at the leading edge of H_{385} and a "zero" at the trailing edge of H_{151} .

Code Preset

In this module, the R/A-D and $\overline{R/A-D}$ signals are buffered for use by the receiver circuits, and $F_L \oplus F_{L/2}$ is buffered for subsystem use. In addition, this module contains the circuits required to generate the signals used in presetting the H- and L-Sequence generators. The event marker signal, EM, as derived by the VHF data demodulator, is used to initiate the generator preset sequence. This signal will effect the preset function only if the code control subsystem is in state T-0. The H-Shift signal will become a "one" in synchronism with the trailing edge of the first H_{256} bit time which occurs when $F_{L/2}$ is "one" and $EM \cdot T-0$ is "one". This signal remains a "one" for as long as the event marker signal is a "one". When the event marker signal goes to "zero", the H-Shift signal will go to "zero" and the H-Sequence will start in either state H_{511} or the "all-zero" state. Due to the fact that the H preset signal began in the last half of an L-Sequence bit, the trailing edge of the EM signal will then define the beginning of an L-Sequence bit. The particular L-Sequence bit is defined by the $EM + L \text{ SYNC}$ signal

which will be a "one" for $(1022/6.4)10^{-6}$ seconds after the trailing edge of the EM signal. Thus, the trailing edge of the EM signal defines within 2 H-Sequence bits the L_{73} to L_{74} bit transition of the transponder L-Sequence generator.

Input Control

The primary function of this module is to serve as a buffer and retiming network for the input signals denoted as A_L , \bar{A}_H , DRC, and Go To T-0.

Associated with each input signal is a two-stage shift register and detector gates such that pulses are formed which are one L-Sequence bit in width occurring in synchronism with the L-Sequence clock rate at "zero" to "one" and "one" to "zero" transitions of each input signal. Input signal \bar{A}_H is inhibited by T-0 to become A_{HI} . That is, A_{HI} is identical to A_H except that it is always "zero" in state T-0. Signal A_{LI} is identical to A_L but delayed in making transitions until L_{120} bit time. $A_L \rightarrow 1$, $A_L \rightarrow 0$, $A_H \rightarrow 1$, and $A_H \rightarrow 0$ are pulses at transitions of A_L and A_H , as defined above, which can occur only during L_{120} bit time. These signals are inhibited by various state signals and used as timing pulses to advance the program state counter and to start the DO and R/A timers.

The R/A Reset signal will be "one" if $A_H \rightarrow 1$ or if the R/A signal is a "one" in states T-1A or T-1B.

The Return To T-0 signal will be a "one" if the Go To T-0 signal goes to a "one" for at least 160 microseconds and if the DO signal is a "one" in state T-1A, or if the R/A signal is a "one" in states T-1A or T-1B.

The remaining signals are self explanatory. Note that the DRC' signal is inhibited in every state except T-2.

Programmer and DO Timer

The programmer is a 5-stage, presetable, shift register which is clocked by the logical "or" function of signals Return To T-0, R/A Set, R/A Reset, DRC . T-2, and ($A_L \rightarrow 1$) (T-0). Each of these pulses will cause the programmer to shift once in accordance with the flow diagram, Figure 6-18. Normally only one stage of the programmer will be set to a "one", and an initial Go To T-0 command will insure this condition. The DO Timer is a 3-stage shift register counter which is normally held in the "all-zero" condition. A DO Set signal will set the first stage to a "one" and the counter will progress through its 7 remaining states to the "all-zero" conditions at the L_{127} rate, unless it is reset by the DO Reset signal.

If the timer reaches the "all-zero" condition before A_{HI} becomes a "one", an output signal denoted by DO will be generated. This signal is a single pulse coincident with the seventh L_{127} pulse after the DO Set signal occurred. This delay will then be 0.123 second.

R/A Timer

In addition to the R/A timer, this module contains the logic required to generate the DO Set and Reset Signals. The DO Set signal is a "one" if $A_L \rightarrow 0$ is a "one" in state T-1A or if $A_H \rightarrow 0$ is a "one" in states T-2 or T-3. The DO Reset signal will be a "one" if $A_H \rightarrow 1$ is a "one" in states T-2 or T-3, or if $A_L \rightarrow 1$ is a "one" in state T-1A. The R/A Timer is identical to the DO Timer except it has seven stages and thus provides a delay of 2.57 seconds before the R/A pulse will occur. This timer will be started if $A_L \rightarrow 0$ is a "one" in state T-1B or if DO is a "one" in states T-2 or T-3. It will be reset by R/A or if A_{LI} is a "one" or if $A_H \rightarrow 1$ is a "one" in states T-1A or T-1B.

The R/A pulse will not be generated if A_{LI} becomes a "one" before 127 L sequence periods have elapsed.

Buffer Module

In this module the timing and state signals required for the formation of the gating signals GC1, GC2, GH1 and GH2 are retimed and buffered. The H-Sequence, L-Sequence, and $F_L \oplus F_{L/2}$ are also buffered for use in the code combiners. In addition, the input Preset signal from which the EM signal is derived is enabled by $\overline{T-0}$ and buffered here.

L_{119} is retimed and buffered for use by the A_L , A_H and Data Demodulator circuits and signal L_{127} is buffered for external use.

L_{2N} is formed as a signal which is a "one" only during the even L sequence bits.

The steering signals for final retiming of the GC1, GC2, GH1 and GH2 gating signals (given in Table VI-2) are formed in this module.

Gate Generator

In this module the final retiming of all gating signals is accomplished, together with the complete formation of the GR and GI gating signals. The retiming delays the gating signals by one H sequence bit from the reference sequence generation. Note that $\overline{GC1}$, $\overline{GC2}$, \overline{GR} and \overline{GI} are the signals furnished to the receiver, and these are the logical inverses of the signals given in Table VI-2. The signal R/A-D is formed in this module and will be a "one" whenever the R/A Timer is running (i.e., for the time between when this timer is set and when it is reset). This signal is also combined with GC1 and GC2 and made available as an output.

Preliminary combination for both the receiver and transmitter codes is accomplished, with Z_R-1 and Z_T-1 denoting these outputs.

Transmitter Combiner

The final transmitter code is formed, retimed and buffered in this module. The transmitter code (TT-Z) form is given in Table VI-2. Note that this code does not contain any F_H component so that retiming by HCL is sufficient. This retiming is accomplished in two stages plus the interface circuits so that the transmitter code is delayed by four cycles of $2F_H$ plus the interface retiming delay from the reference sequence generation. A 6.4 MHz square wave, denoted by F_{HS} , is supplied for external use, and is equivalent to F_H delayed by the interface retiming delay. In addition, some retiming and combining required for the receiver code is accomplished in this module resulting in the two partial receiver codes Z_R-2 and Z_R-3 . Note that Z_R-2 has a delay of 2 cycles of F_H while Z_R-3 has a delay of 4 cycles of F_H .

Receiver Combiner

The final receiver code is formed, retimed, and buffered in this module. This code contains F_H as a component and must be retimed with $2F_H$ after this component is added. The final code form is given in Table VI-2 and is delayed from the reference sequence generation by six cycles of $2F_H$ plus the interface retiming delay. Retiming of all components of the code is required to insure the proper phase relationships among the components in the final code.

State signal T-0 is buffered to three outputs for external use.

The remainder of the logic is required to set and reset the R/A Timer module at the proper times in states T-1A and T-1B.

The following list of input and output signals of the code control, gives a characteristic description of each.

Inputs

1. $T-2f_H$ - a 12.8 MHz square wave, 0.30v $\pm 10\%$ p-p.
2. T-DATA - a digital waveform which may have transitions at L_{127} and L_{59} .
3. T-GO TO T-0 - a DC level signal; std. digital level.
4. T-DRC - a DC level signal; std. digital level.
5. $T-\overline{\text{PRESET}}$ - a DC level signal std. digital level.
6. $T-A_L$ (AMPL) - a series of reversible polarity 10 μsec wide pulses occurring at L_{119} time and variable in amplitude from 0 to 5v p-p.
7. $T-A_H$ (AMPL) - a series of reversible polarity 10 μsec wide pulses occurring at L_{119} time and variable in amplitude from 0 to 5v p-p.

Outputs

1. $T-L_{127}$ (C/O)
 $T-L_{127}$, E
 $T-L_{59}$ Pulse waveform; standard digital voltage levels; pulse width - $2044 \div 2f_H$; pulse repetition frequency - $2f_H \div 259588$.
 2. $T-A_L$ (C/O)
 $T-A_H$ (C/O)
 $T-A_H$ D-C level; standard digital voltage levels; must make transitions within 70 μsec after leading edge of L_{119} pulse; $T-A_L$ (C/O) will be a "1" if $T-A_L$ (AMPL) is more negative than -1.0 volt and will be a "0" if $T-A_L$ (AMPL) is more positive than -0.4 volt; $T-A_H$ (C/O) and $T-A_H$ will be a "1" if $T-A_H$ (AMPL) is more negative than -1.0 volt and will be a "0" if $T-A_H$ (AMPL) is more positive than -0.4 volt.
- $T-\overline{A_L}$ Logical inverse of above.
- $T-\overline{A_H}$ (3 places)

3. T-0, E₁
T-0, E₂
T-0, E₃
T-1A, E
T-2, E
T-3, E
T-1B, E
 $\overline{\text{T-0}}$, E
D-C level; standard digital voltage levels; must make transitions at trailing edge of the $F_L \oplus F_{L/2}$ signal.

Logical inverse of above.
4. T-F_{HS}
Square wave; frequency - f_H , signal levels - logic "1" = +0.30v \pm 0.05v, and logic "0" = 0.00v \pm 0.03v; rise time - less than 5 nsec; noise level - less than 50 millivolts either level.
5. T-R/A-D(v)
D-C level; standard digital voltage levels; must make transitions at leading edge of L₁₂₀ or L₁₂₇.

T- $\overline{\text{R/A-D}}$ (v) Logical inverse of above.
6. T- $\overline{\text{G}_{C1} \cdot \text{R/A-D}}$
T- $\overline{\text{G}_{C2} \cdot \text{R/A-D}}$
Logic "0" of standard digital voltage level or pulse waveform; standard digital voltage levels; pulse width - $511 \div 2f_H$; pulse repetition frequency - $2f_H \div 2044$ or $2f_H \div 4088$.
7. T-DR-A_L
Pulse waveform; standard digital voltage levels; pulse width - $2044 \div 2f_H$; pulse repetition frequency - $2f_H \div 259588$.
8. T-DR-G_{H1}
T-DR-G_{H2}
Pulse waveform, standard digital voltage levels; pulse width - $511 \div 2f_H$; pulse repetition frequency - $2f_H \div 2044$ or $2f_H \div 4088$. NOTE: Signals are Logic "0" during L₁₁₉.

9. $T-\overline{G}_{C1}$
 $T-\overline{G}_{C2}$ Pulse waveform; standard digital voltage levels; pulse width - $511 \div 2f_H$; pulse repetition frequency - $2f_H \div 2044$ or $2f_H \div 4088$.
10. $T-\overline{G}_R$ Pulse waveform; standard digital voltage levels, pulse width - $511 \div 2f_H$; pulse repetition frequency - $2f_H \div 2044$ or pulse width - $1022 \div 2f_H$; pulse repetition frequency - $2f_H \div 4088$.
11. $T-\overline{GI}$ Logic "0" of standard digital voltage level or pulse waveform; standard digital voltage levels; pulse width - $1022 \div 2f_H$; pulse repetition frequency - $2f_H \div 2044$.
12. $TR-Z$ A pseudo-noise coded waveform (code description given below); frequency - f_H bits per second; signal levels - logic "1" = $+0.30v \pm 0.05v$ and logic "0" = $0.00v \pm 0.03v$; rise time - less than 5 nsec; noise level - less than 50 millivolts either level.

6.5.3 Doppler Inverter

The Doppler Inverter connects the Tracking Transmitter Frequency Synthesizer to the Tracking Receiver Carrier loop VCO and in doing so performs a frequency translation.

A positive Doppler offset at the receiver VCO is coherently converted to a negative Doppler offset with the carrier frequency preserved.

$$f_o \pm f_D \xrightarrow{\text{invert}} f_o \mp f_D$$

Retransmission of this signal results in the Vehicle receiving a frequency with essentially no Doppler shift from the signal it transmitted.

To achieve full coherency of signals the Vehicle instructs the Doppler Inverter to sweep to true Doppler so that the Vehicle receives a signal with two way Doppler present.

Inversion of the Doppler offset is accomplished by the process shown in Figure 6-33. The $2/3 F_o$ source is phase locked to the station clock. Doppler is preserved in the lower sideband output of the first mixer, but is reversed in the lower sideband of the second mixer due to the change in sign.

It is seen, also from Figure 6-33, that if F_o has the Doppler added and becomes $2/3 (f_o + f_D)$, then true Doppler is preserved at the output of the second mixer.

The $2/3 f_o$ signal is fed from the phase locked oscillator of the Tracking Filter shown in Figure 6-34.

The tracking filter may be locked to either the station clock multiplied to 19.2 MHz or the 19.2 MHz coherent derivative of the Tracking Receiver local oscillator. Figure 6-35 shows the method of connection.

It is necessary to assist the acquisition of the Tracking Filter loop, and to control the rate of sweep when transferring from Reverse-to-Track modes of operation. The Doppler Sign Detector compares the phase of the beat notes from the phase detector and the coherent amplitude detector. The comparison results in the application of a voltage pulse to a summing port of the differential amplifier driving the control filter. This voltage will be of the correct polarity to drive the VCO to the input frequency.

The sign detector is shown in Figure 6-36. The beat note outputs from the phase detector and CAD will always be approximately 90 degrees out of phase with each other. If, as shown in the diagram, the output of the phase detector lags that of the CAD, the input to the Tracking Filter is above the reference frequency being generated by the loop VCO. The shaper output for the phase detector will be transferred to the register output by the negative-going transition of the CAD shaper output. The "1" state of the

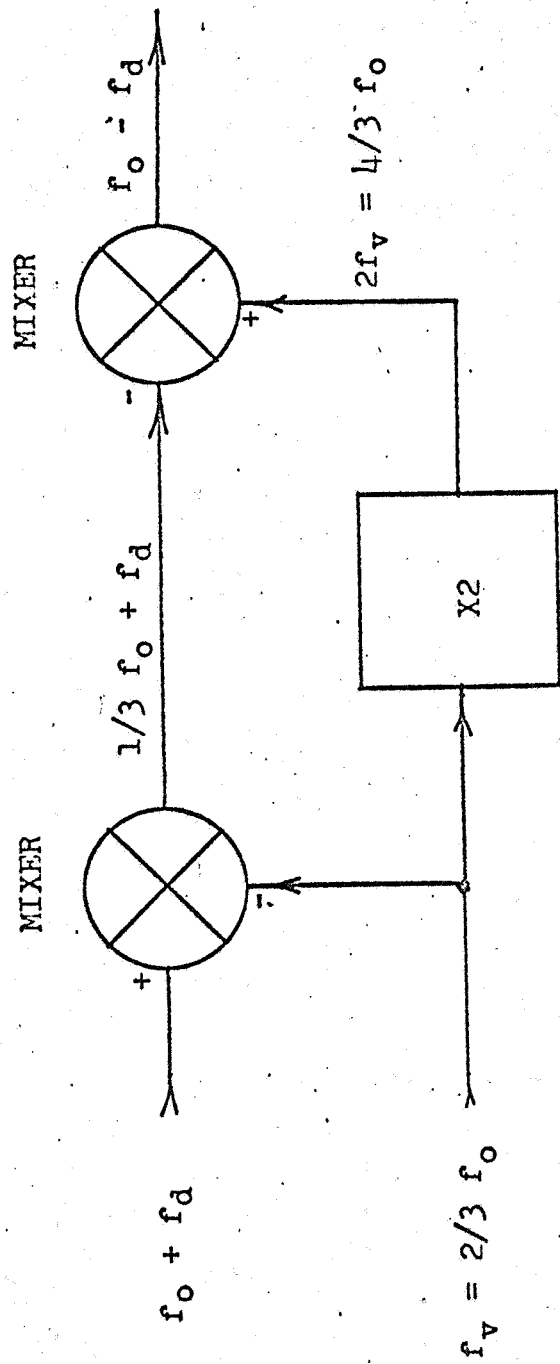


Figure 6-33. Doppler Inversion

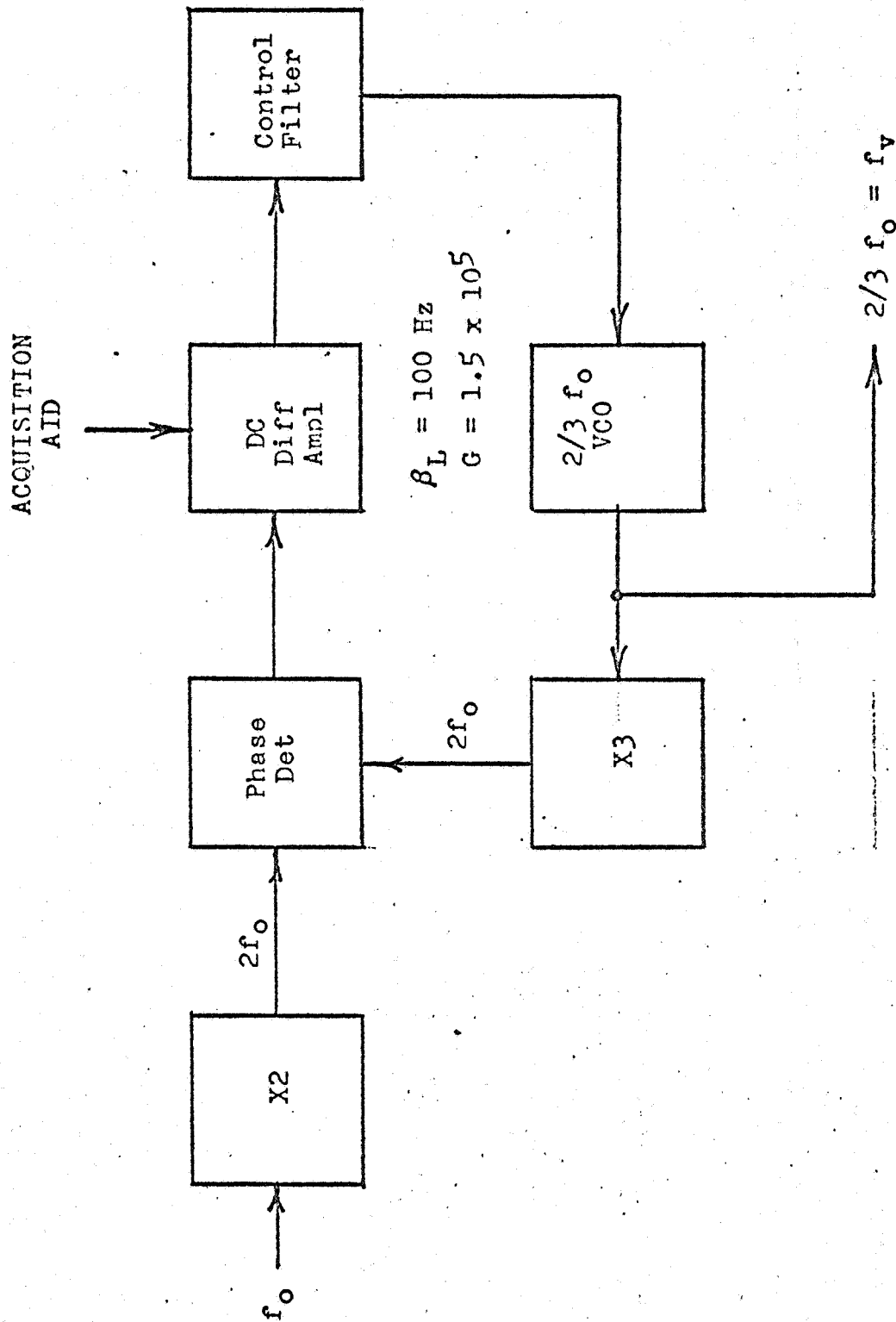


Figure 6-34. Tracking Filter

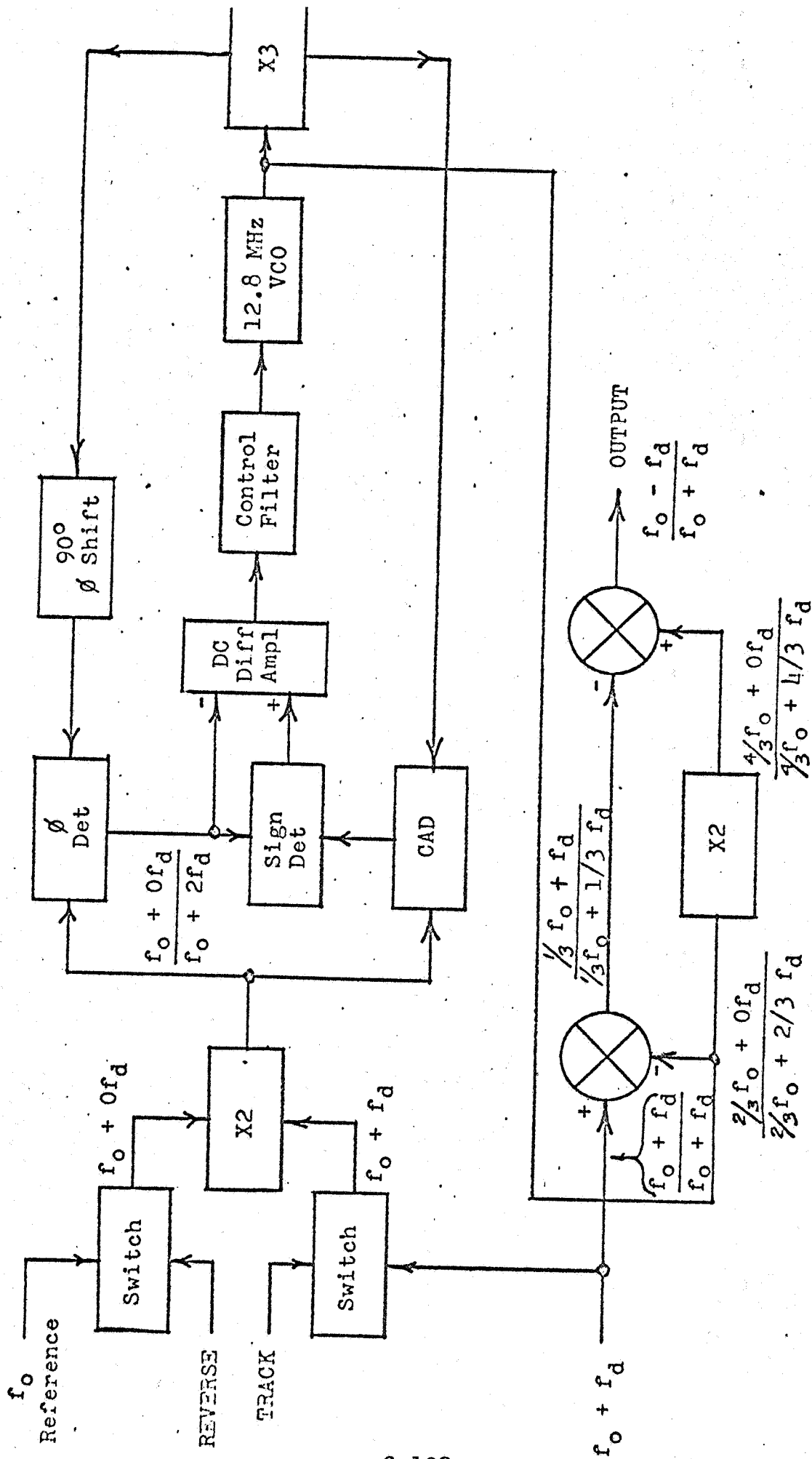


Figure 6-35. Doppler Inverter

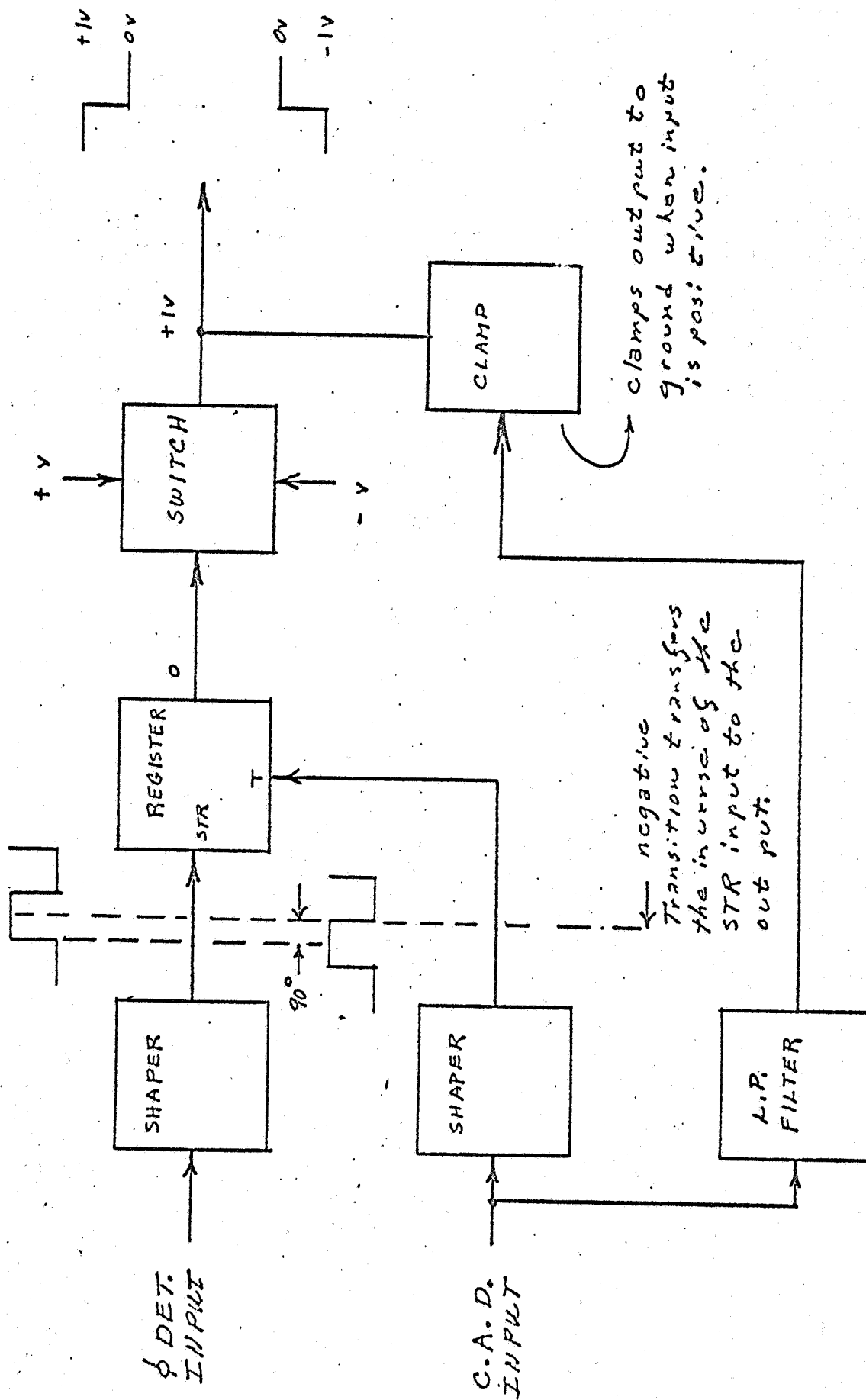


Figure 6-36. Doppler Sign Detector

register output switches a negative voltage to the output, raising the VCO frequency, while the "0" state gives a positive voltage.

Referring to Figure 6-35, when the input is switched from REVERSE to TRACK, we switch from the Reference (f_o) to the VCO ($F_o + f_D$) source. The tracking filter, assisted by the sign detector must acquire the new source. The fixed sign detector output is applied, through a fixed gain to the loop filter which integrates the step change in voltage to sweep the VCO, and the inverter f_o output to the $f_o + f_D$ frequency.

When the new signal is acquired, the positive voltage from the CAD operates the clamp and shorts the sign detector output to ground.

6.5.4 Transmitter Synthesizer

The basic function of the synthesizer is to provide a transmitter source of the proper frequency which is phase coherent to the tracking receiver VCO. This is accomplished in modules 1A2A14, 1A2A15 and 1A2A17 which comprise a Type I second order phase locked loop. A functional block diagram of the loop is shown in Figure 6-37.

The 19.2 MHz signal from the Doppler Inverter is the reference to which the transmitter VCO's are locked. The L-band output of the transmitter may be required to be any frequency from 1750 to 1850 MHz selected in 400 kHz steps. Each transponder has four selectable transmitter channels. The range of the VCO's will correspondingly be 27.3 to 28.9 MHz selectable in 6.25 kHz steps.

The 19.2 MHz reference is split into two paths, with one being fed to a $\div 48$ which provides a 400 kHz reference for a digital exclusive OR phase detector. The other is mixed with the 28 MHz VCO to provide a nominal 9 MHz signal which is fed to a digital programmable divider. The divider is controlled by the Station Control Receiver and selects the proper division ratio to divide the 9 MHz signal to 6.25 kHz. This signal is then multiplied by

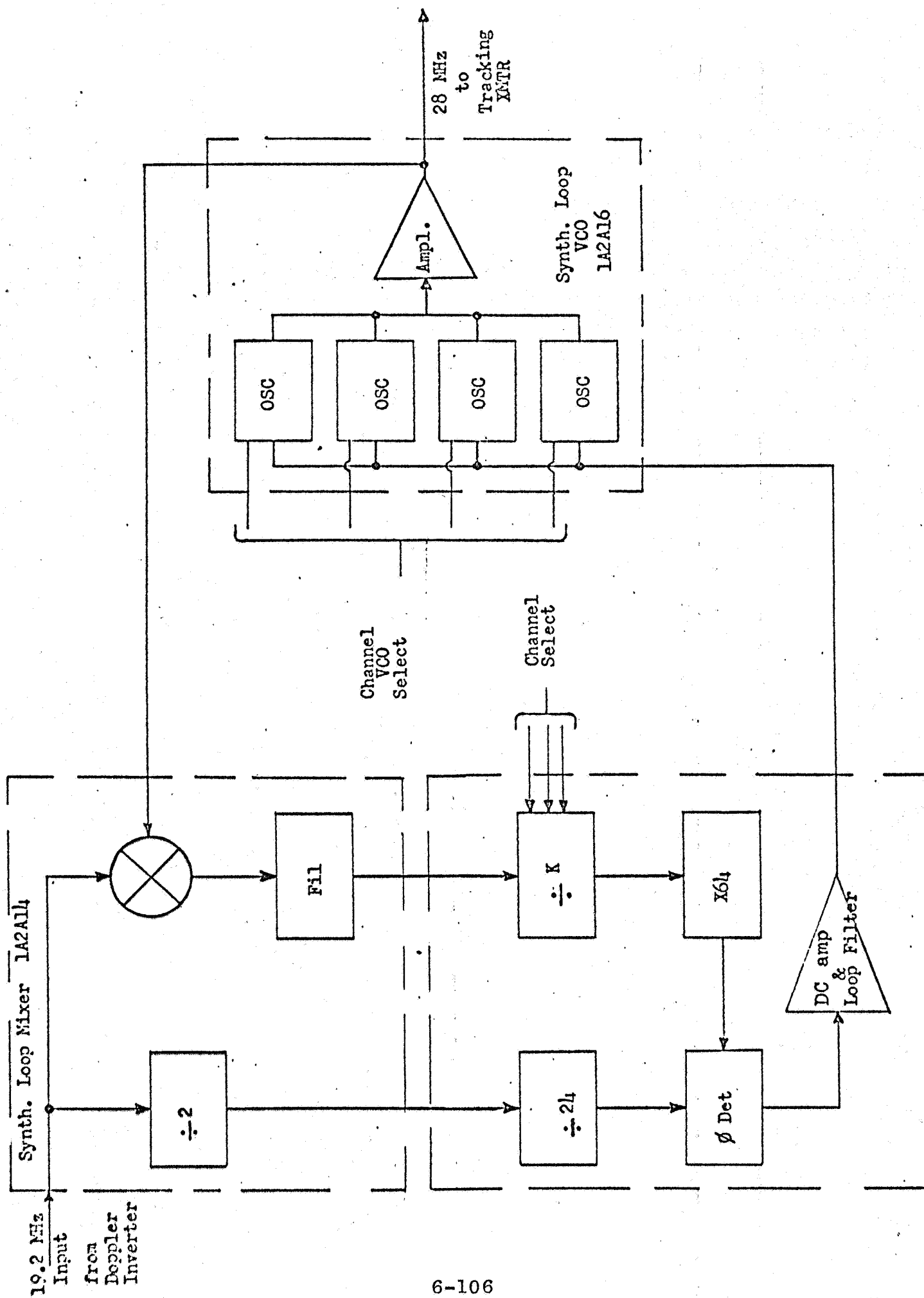


Figure 6-37. Functional Block Diagram Tracking Transmitter Frequency Synthesizer

64 to provide a 400 kHz signal to the phase detector and loop filter which follows. This control from the loop filter is then fed to the synthesizer oscillators thus closing the loop.

The correct oscillator is instructed ON at the same time that the dividers are being programmed.

The synthesizer loop has a loop gain of 6400 sec^{-1} and 28_L of 200 Hz which allows the loop to acquire the reference with its full Doppler component and to track the Doppler sweep.

Figure 6-38 is a simplified diagram of the loop and an explanation of the loop frequency relationships.

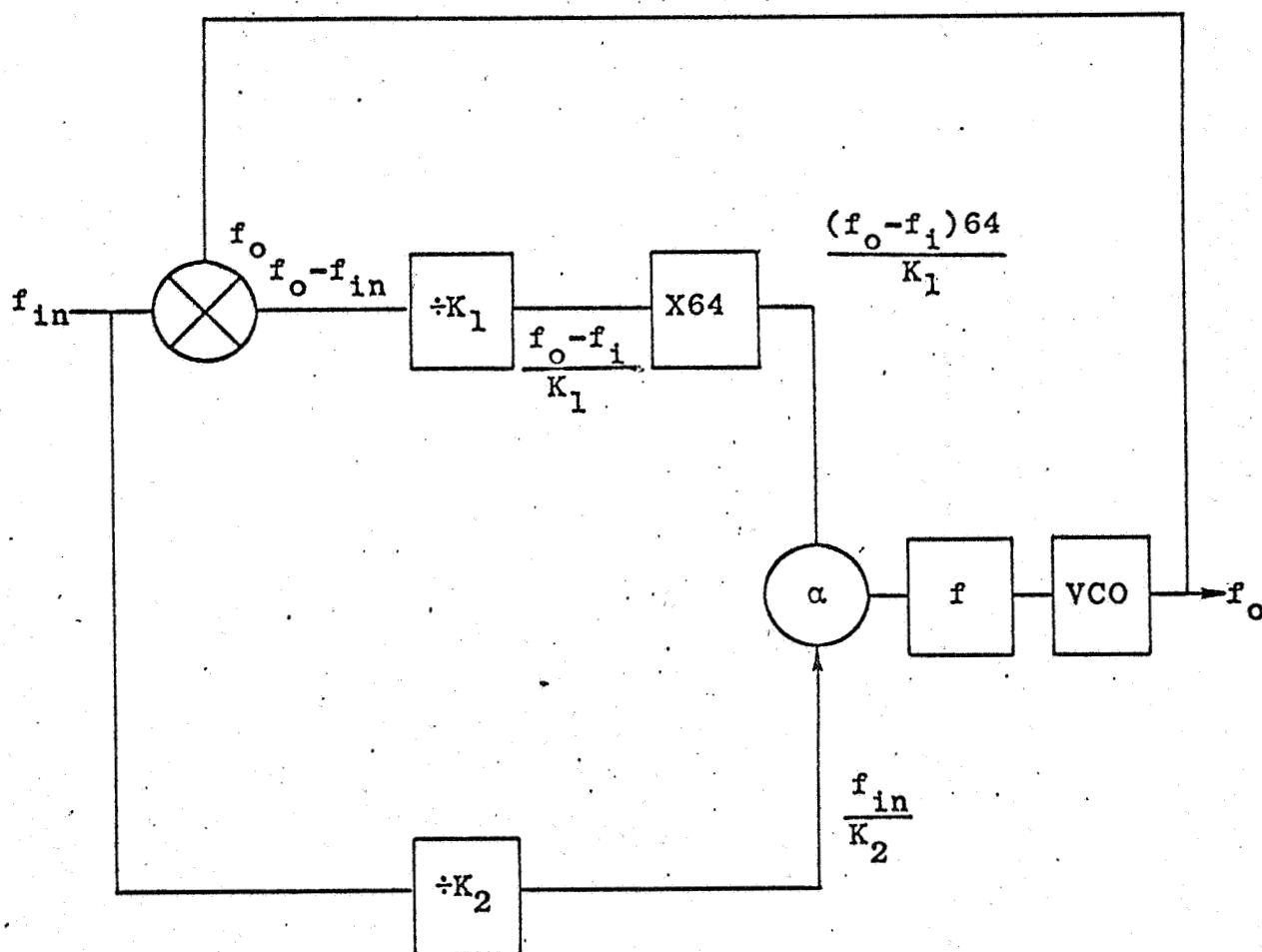


Figure 6-38. Synthesizer Loop

For a locked loop condition the signals at the input to the phase detector must be equal in frequency.

$$64 \frac{(f_o - f_{in})}{K_1} = \frac{f_{in}}{K_2}$$

Rearrange terms:

$$\frac{f_o}{f_{in}} = \frac{K_1}{64 K_2} + 1$$

Substituting values

$$K_2 = 48, f_{in} = 19.2 \text{ MHz}$$

$$f_o = 19.2 \left(\frac{K_1}{3072} + 1 \right)$$

For any required transmitter frequency, the VCO (F_o) can be determined by dividing by the transmitter multiplication (X64). Then the value of K_1 can be determined by:

$$k_1 = \left(\frac{f_o}{19.2} - 1 \right) 3072$$

6.5.5 Tracking Transmitter

The Tracking Transmitter consists of two modules 1A2A17 and 1A2A18 which provide the multiplication and modulation of the transmitter carrier. 1A2A17 consists of a X2 multiplier, an auxiliary phase modulator and filter amplifier. The phase modulator, used mainly for test purposes has a constant modulation response +0, -3 db from 50 Hz to 100 kHz and linear with 5 percent for modulation indices up to 0.125 radian at the output of the module. 1A2A18 consists of a X4 multiplier, wideband biphasic modulator at 224 MHz and transistor amplifier and X2 multiplier which provides a nominal 100 mw at 448 MHz. This signal drives the X4 multiplier which is a wideband step recovery diode device. The X4 provides a nominal 10 mw, 1800 MHz signal which is fed to the TWT for amplification to 10 watts. The wideband modulator is

a hot carrier diode device with rise time on the order of 5 nsec. The modulator actually shifts the phase ± 11.25 degrees at the carrier frequency of 224 MHz with an accuracy of about $1/4$ degree. The resultant modulation at L-band is therefore biphase.

The TWT is a Hughes 1122A tube. It has a self contained power supply and operates from a 110 VAC 60 Hertz power source.

A functional block diagram of the transmitter is shown in Figure 6-39.

6.6 POWER AMPLIFIER (1A3)

The power amplifier contains circuits to switch power supplies for the tracking receiver (1A2) and to switch prime power to an auxiliary output. The switching circuit consists of two relays and a driving circuit which receives commands from the control receiver (1A1). Both relays are open when the station is "OFF." Arrival of a "one" at the driver circuit energizes relay K_1 , which applies +28 VDC to relay K_2 and the four DC/DC converters. Figure 6-40 shows the functional paths. The mounting plate of the power amplifier drawer has two thermal switches which turn on a blower when plate temperature reaches 45°C .

6.7 POWER CONVERTER (1A4)

The power converter is a commercial unit with the following Motorola modifications: A110/220 VAC 5 AMP circuit breaker was mounted in an opening cut in the front panel. An A-C line cord was passed through the rear panel and routed to the breaker. The line from the breaker output was returned to the rear and connected internally to the barrier strip on the rear panel. For theory of operation refer to the manual of the power converter, Mid-Eastern Electronics Model 652-07.

Aux. Phase Mod. Input

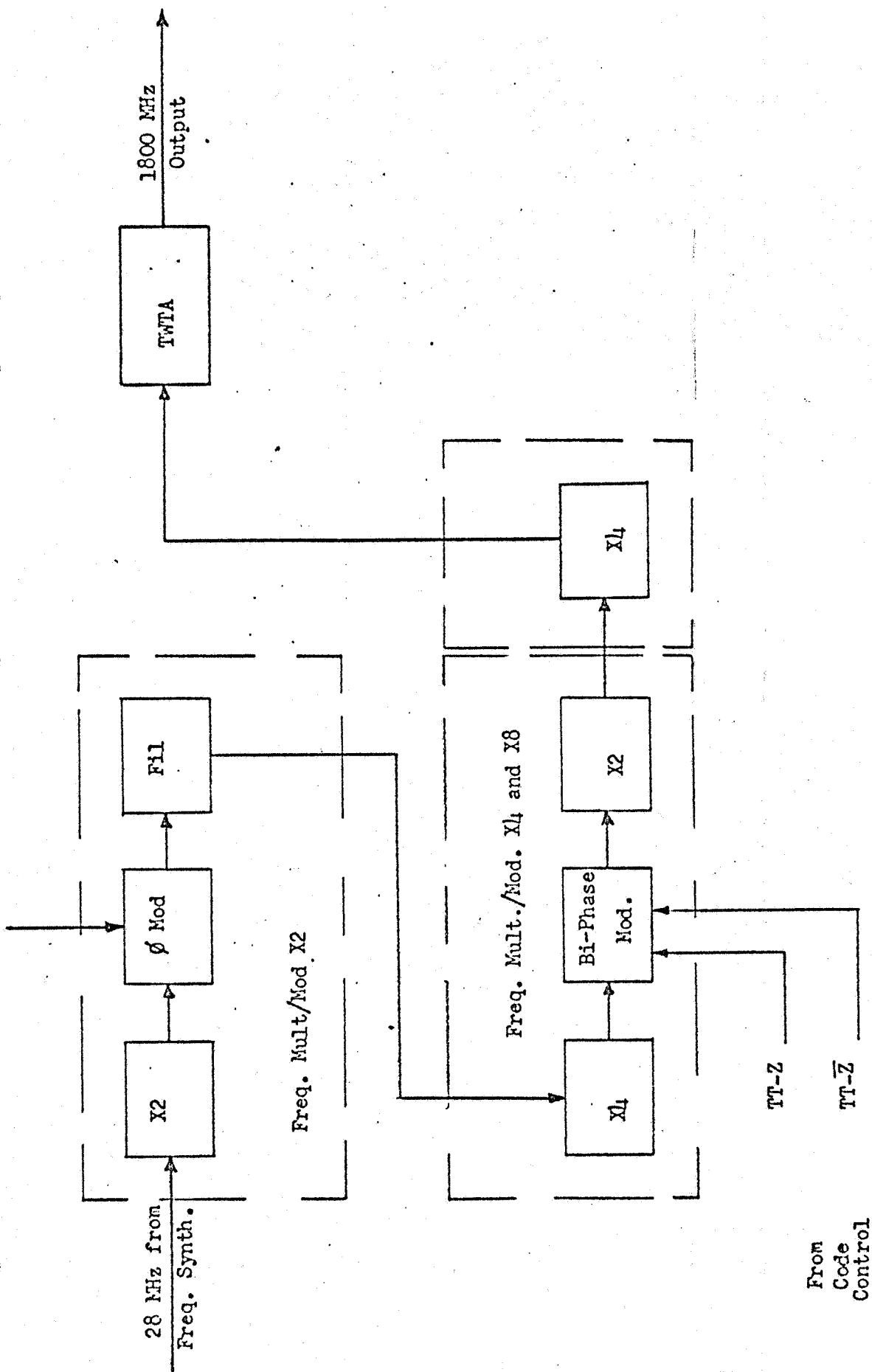


Figure 6-39. Functional Block Diagram Tracking Transmitter

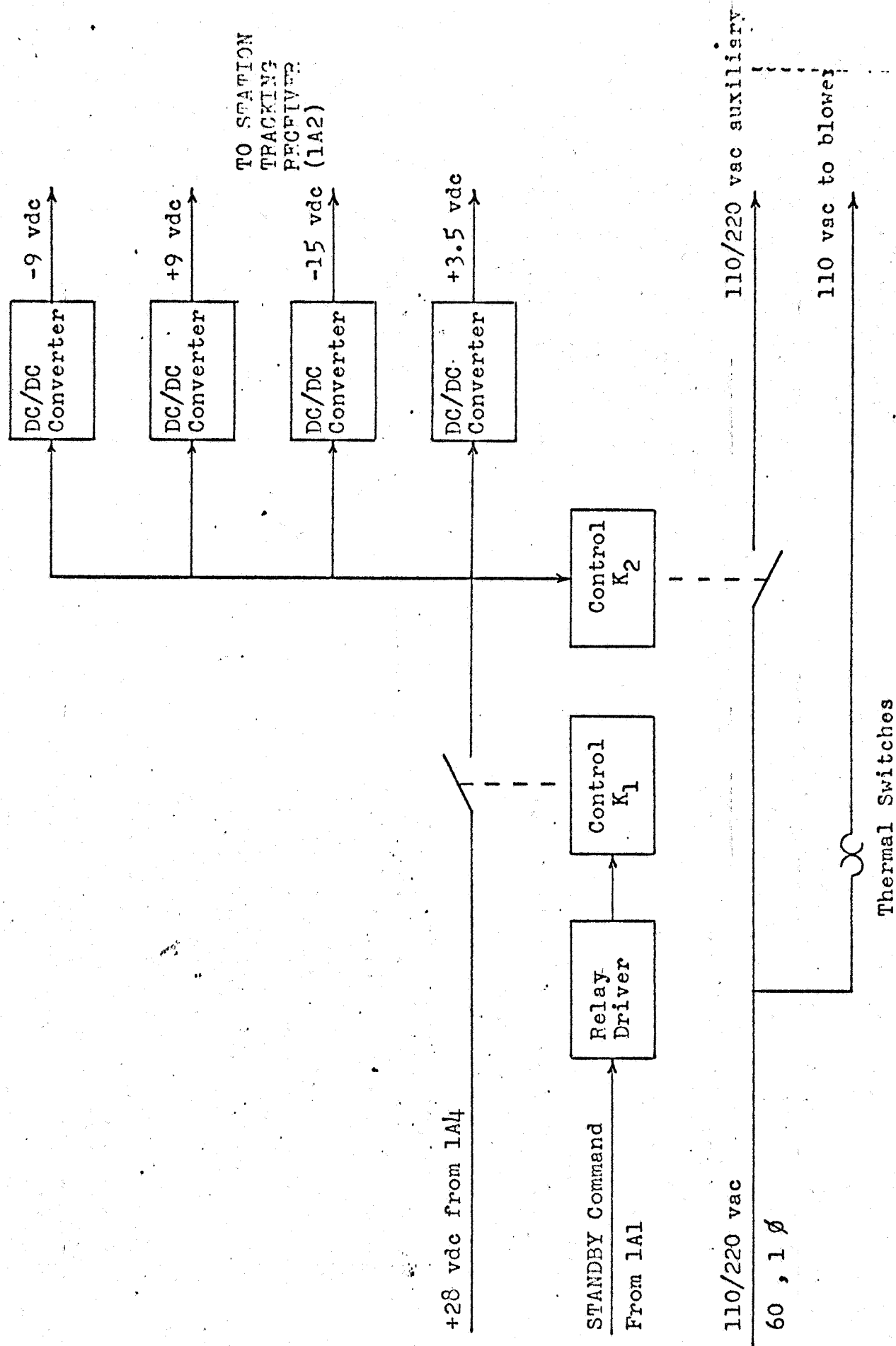


Figure 6-40. Power Amplifier

SECTION VII

7. AROD VEHICLE CHECKOUT EQUIPMENT

7.1 PURPOSE OF THE EQUIPMENT

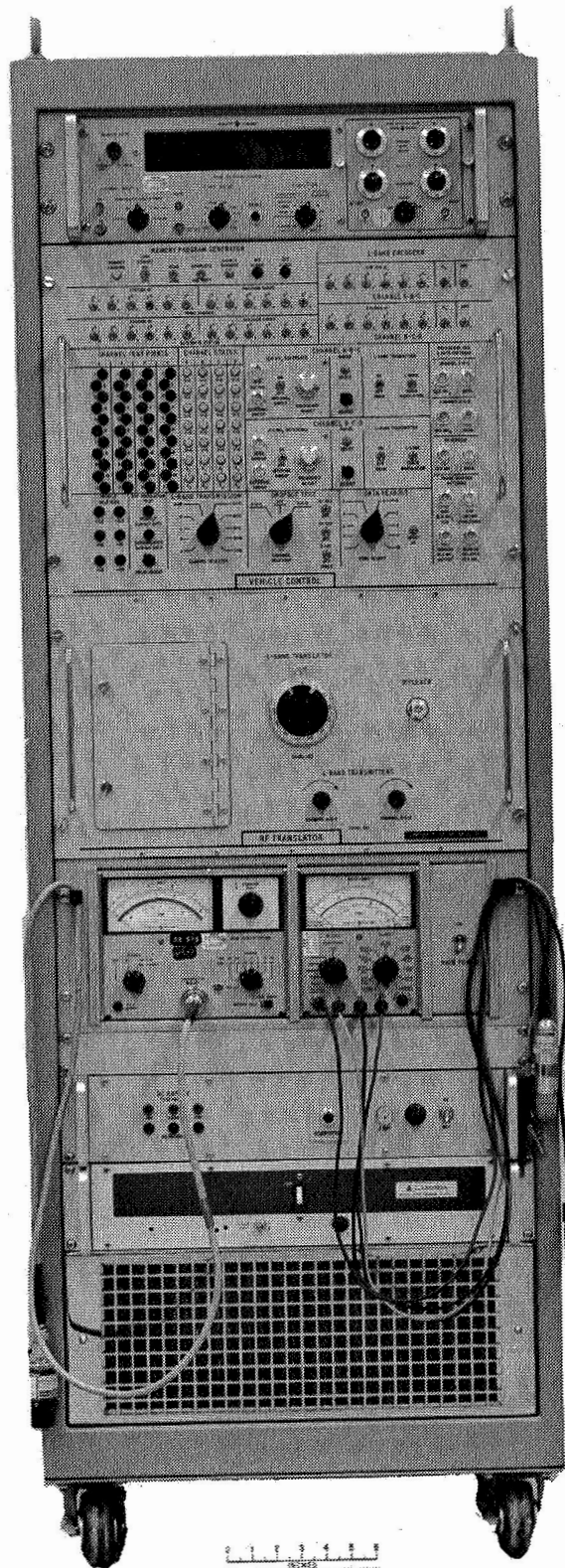
The AROD Vehicle Checkout Equipment provides a test facility for the AROD Vehicle-Borne System. It is intended to exercise, at least, all functions of the system, and to evaluate various aspects of operation to a fine degree. It will also serve as a maintenance tool for troubleshooting the Vehicle-Borne System.

7.2 PHYSICAL DETAILS

Physical details of the Vehicle Checkout Equipment are shown in figure 7-1, a front view and figure 7-2, a rear view. The rack is a 5-foot standard 19-inch cabinet which contains several major assemblies. The Vehicle Control Drawer (1A1) and the R-F Translator (1A2) are mounted on slides with cable retractors to permit operation in an open position. Power supplies required for V-C/O Equipment operation (± 9 v, ± 3.5 v) are contained in 1A3 whereas 1PS1 supplies prime power for the Vehicle-Borne System. Commercial assemblies included in the rack are a frequency counter and time interval meter (HP-5245L with 5262A plug-in), a power meter (HP-431B), a V-O-M (HP-412C) and a blower assembly. Other commercial equipment supplied with the V-C/O Equipment are a spectrum analyzer (HP-851B/8551B), oscilloscope (Tektronix 585A), and a digital printer (HP-562A). A 115 volt AC distribution strip is included in the rear of the rack for these auxiliary instruments. Identification of the major subassemblies is tabulated in table 7-1.

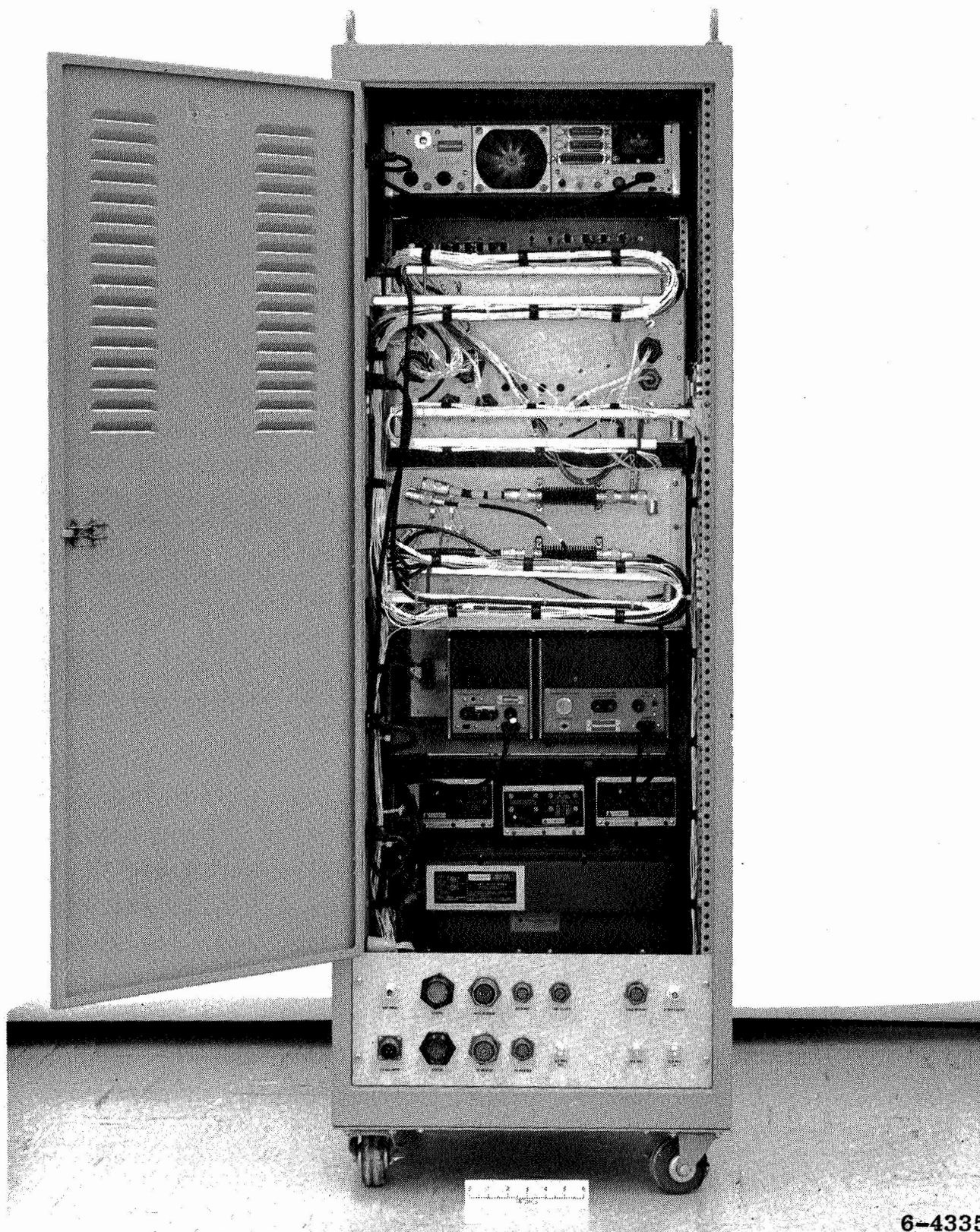
7.3 ASSEMBLY DESCRIPTION

All components of the rack are panel-mounted except 1A1 and 1A2 drawers which are slide mounted.



6-4334

Figure 7-1. AROD Vehicle Checkout Equipment, Front View



6-4335

Figure 7-2. AROD Vehicle Checkout Equipment, Rear View

TABLE 7-1. Rack-Mounted Assemblies

| Assembly Name | Part or Model No. | Manufacturer | Ref. Desig. |
|-----------------------|-------------------|-----------------|-------------|
| CABINET ASSEMBLY | 16-22619H01 | Motorola | |
| VEHICLE CONTROL DWR | 01-22467H01 | Motorola | 1A1 |
| R-F Translator DWR | 01-22468H01 | Motorola | 1A2 |
| POWER SUPPLY, V-C/O | 79-28467H01 | Motorola | 1A3 |
| POWER SUPPLY, VEHICLE | LM-F28 | LAMBDA | 1PS1 |
| FREQUENCY COUNTER | 5245L | Hewlett-Packard | |
| TIME INTERVAL UNIT | 5262A | Hewlett-Packard | |
| POWER METER | 431B | Hewlett-Packard | |
| VOLT-Ohm-MILLIAMETER | 412C | Hewlett-Packard | |
| BLOWER ASSEMBLY | 300 CFM-700-875 | Stone & Smith | |
| AUXILIARY EQUIPMENT | | | |
| SPECTRUM ANALYZER | 851A/8551A | Hewlett-Packard | |
| OSCILLOSCOPE | 585A | Tektronix | |
| DIGITAL PRINTER | 562A | Hewlett-Packard | |

7.3.1 Vehicle Control Drawer (1A1)

The 1A1 drawer is shown in figure 7-3 and the drawer layout in figure 7-4. It contains two bays, each basically a transponder simulator. Each bay contains 4 R-F type modules and 5 digital type modules. Transponder simulator #1 consists of A5, A7, A9, A11, A13; simulator #2 consists of A6, A8, A10, A12, and A14. Modules A3, A4, and A18 provide functions common to both simulators. Modules A15, A16 and A17 provide a means for loading and reading the Vehicle Memory. Modules A19 and A20 are used to drive the front panel display lamps. Module A21 is a commercial "Variogon" phase shifter built to operate at 12.8 MHz. Shielding is provided between bays, between the digital and r-f sections of the drawer, and on the bottom, between the R-F sources for the digital and the R-F modules. Table 7-2 presents a listing of components of the Vehicle Control drawer.

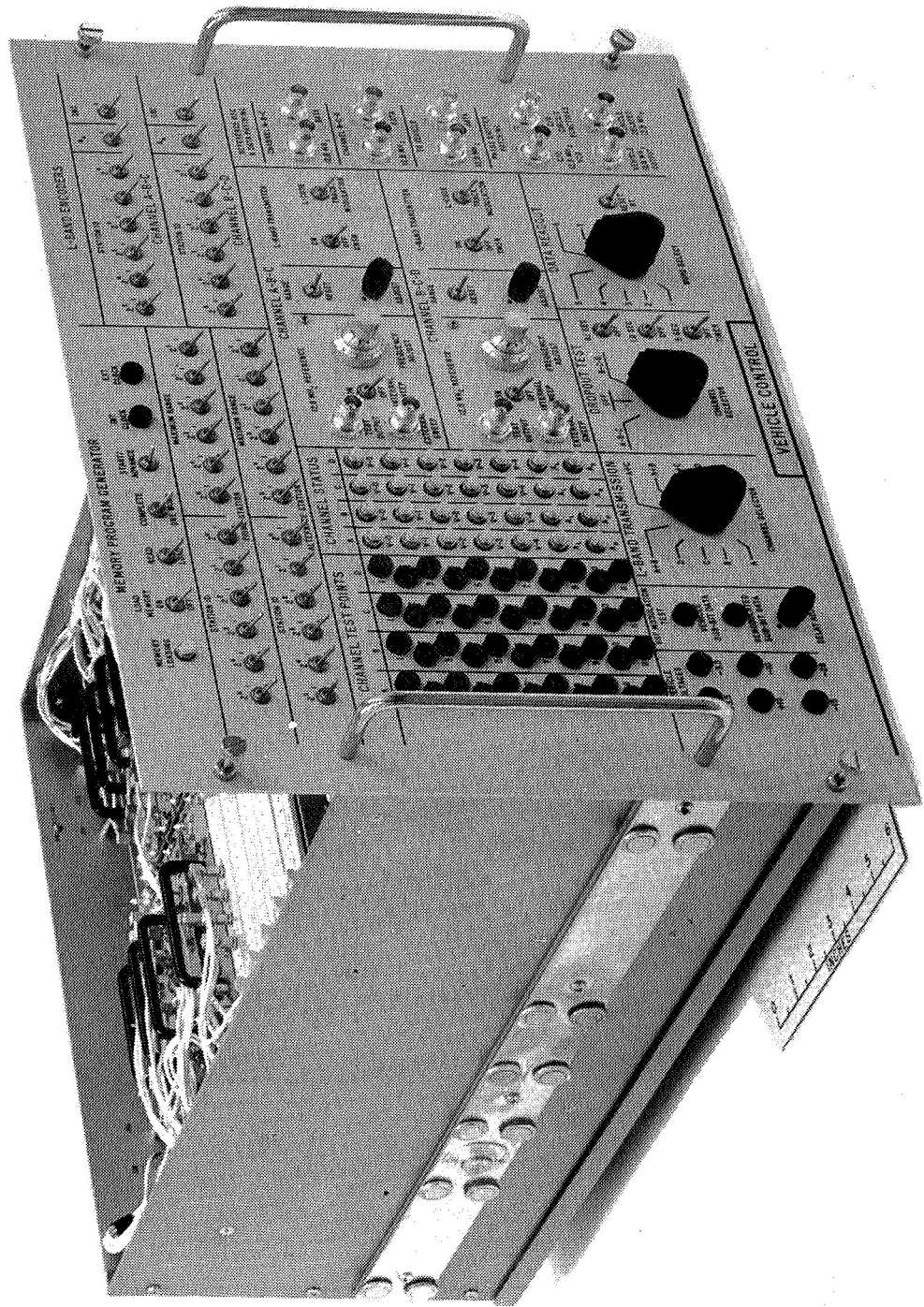


Figure 7-3. Vehicle Control Drawer

6-4340

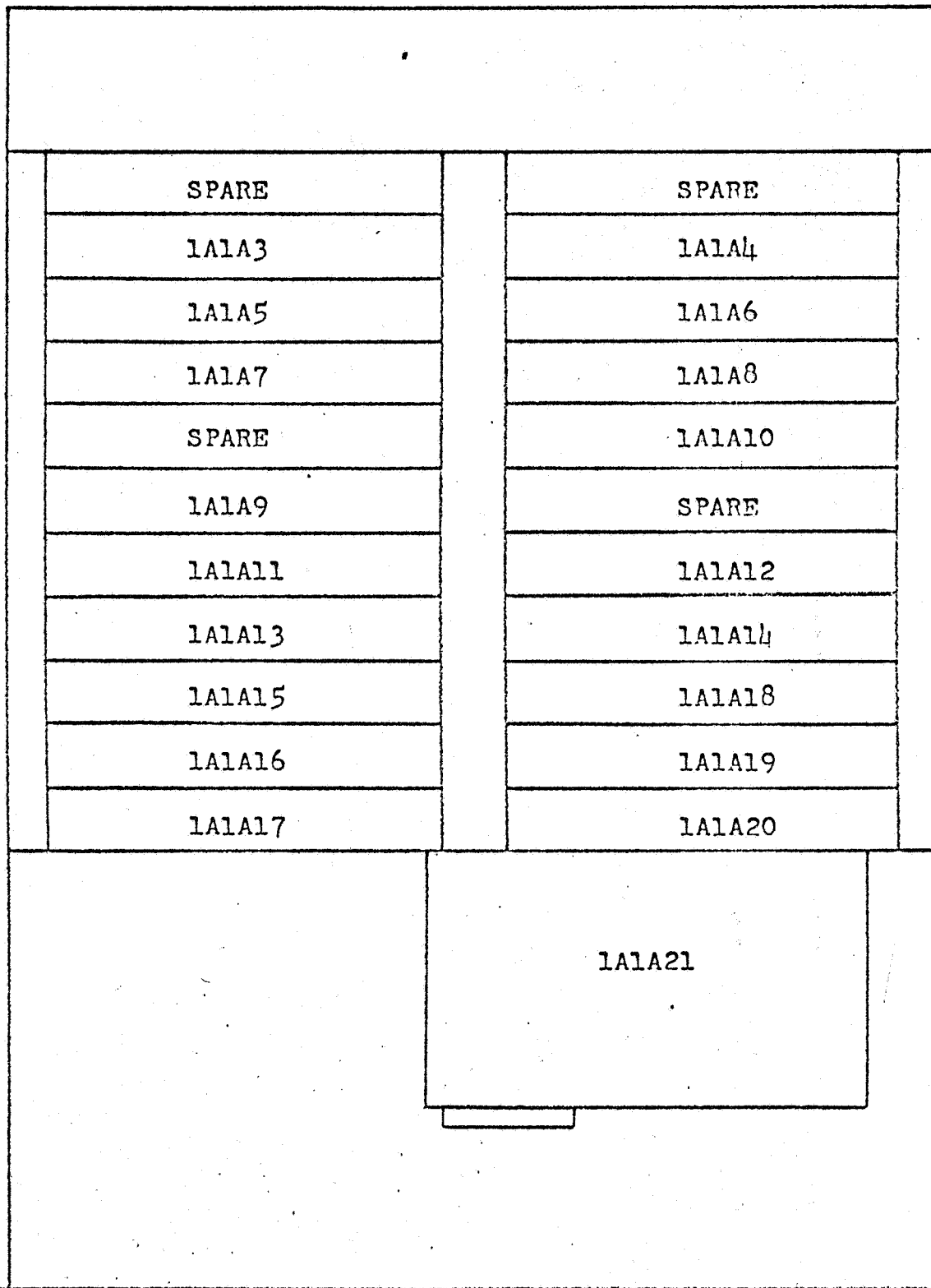


Figure 7-4. Vehicle Control Drawer Layout, Top View

TABLE 7-2. Components of Vehicle Control Drawer

| Module | Title | Part No. | Manufacturer |
|--------|-------------------------|-------------|-----------------|
| 1A1A3 | H. F. Mixer | 01-22488H01 | Motorola |
| 1A1A4 | VHF Demodulator | 01-22663H01 | Motorola |
| 1A1A5 | Channel VCO's | 01-22688H01 | Motorola |
| 1A1A6 | Channel VCO's | 01-22688H01 | Motorola |
| 1A1A7 | Reference VCO | 01-22694H01 | Motorola |
| 1A1A8 | Reference VCO | 01-22694H01 | Motorola |
| 1A1A9 | Frequency Dividers | 01-22444H01 | Motorola |
| 1A1A10 | Frequency Dividers | 01-22444H01 | Motorola |
| 1A1A11 | Code Control Unit | 01-26384G01 | Motorola |
| 1A1A12 | Code Control Unit | 01-26384G01 | Motorola |
| 1A1A13 | Data Encoder | 01-26381G01 | Motorola |
| 1A1A14 | Data Encoder | 01-26381G01 | Motorola |
| 1A1A15 | Memory Prog. Gen. | 01-26390G01 | Motorola |
| 1A1A16 | Memory Data Clock | 01-26392G01 | Motorola |
| 1A1A17 | Memory Prog. Control | 01-26394G01 | Motorola |
| 1A1A18 | Time Pulse Generator | 01-26387G01 | Motorola |
| 1A1A19 | Lamp Driver | 01-29197G01 | Motorola |
| 1A1A20 | Lamp Driver | 01-29197G01 | Motorola |
| 1A1A21 | Variogon. Phase Shifter | V56A52 | Nilsen Mfg. Co. |

7.3.2 R-F Translator (1A2)

The 1A2 drawer shown in figure 7-5 contains the higher frequency circuitry (138, 1800, and 2214 MHz). It is a fully shielded, R-F tight enclosure. The internal portions of the drawer are compartmented to provide shielding between the various functions. The VHF (138 MHz) circuitry and the supply distribution are in separate compartments on the bottom of the chassis. Separate compartments are provided in the top section for the calibrated attenuator and for housing the three R-F type modules. The latter are (2) multipliers, X16 (28.1 to 450 MHz) for the two transponder simulators, and a multiplier, X64 (6.4 to 414 MHz) for the 2214 to 1800 MHz translator. Table 7-3 presents a listing of major components of the R-F Translator.

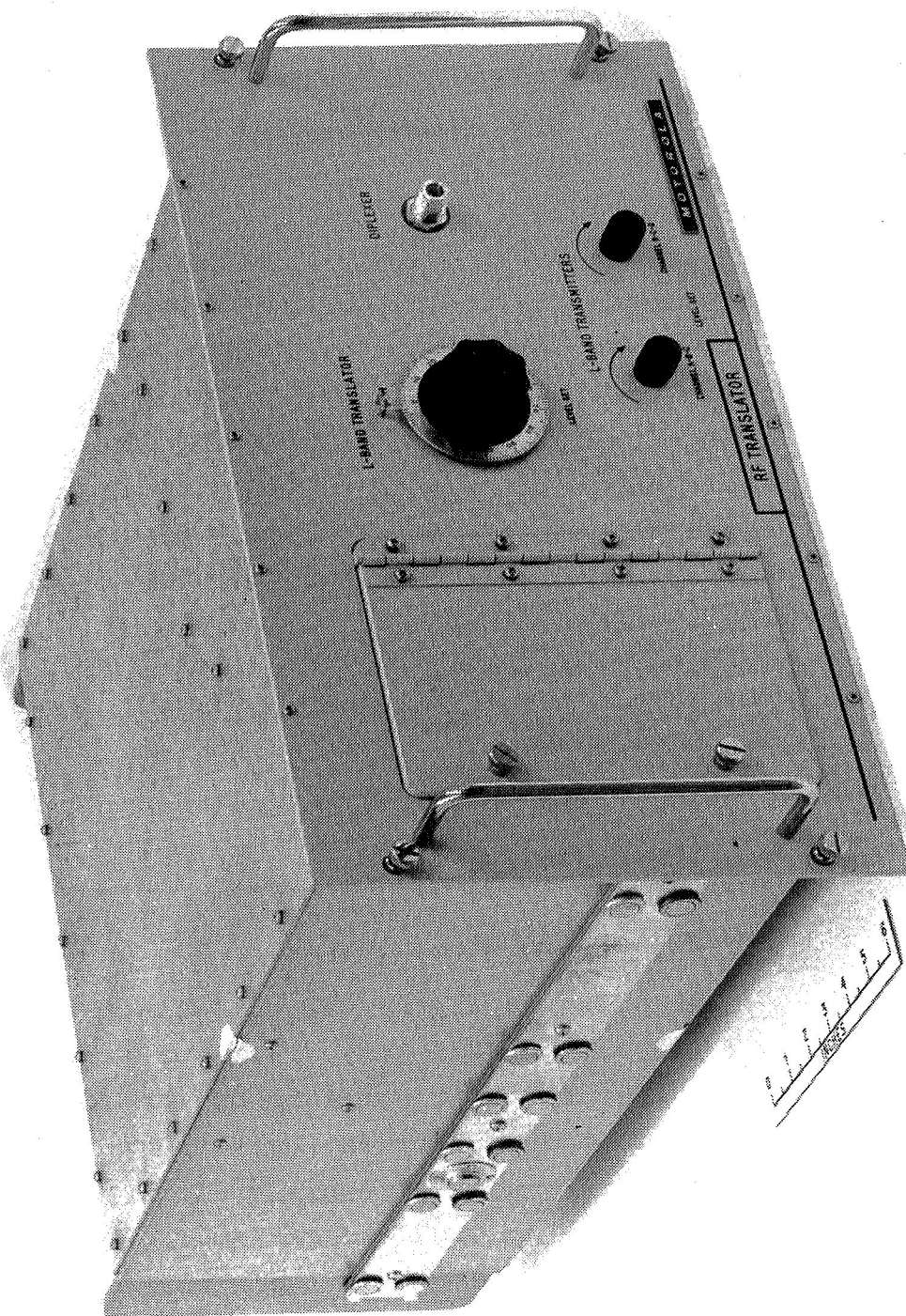


Figure 7-5. R-F Translator Drawer

6-4339

TABLE 7-3. Components of R-F Translator Drawer

| Module | Title | Part No. | Mfr. |
|--------|-------------------------|-------------|-----------|
| 1A2A1 | Mult. X16, Biphase Mod. | 01-22594H01 | Motorola |
| 1A2A2 | Mult. X16, Biphase Mod. | 01-22594H01 | Motorola |
| 1A2A3 | Multiplier X64 | 01-22673H01 | Motorola |
| 1A2A4 | Multiplier X4 | 01-28469H01 | Motorola |
| 1A2A5 | Multiplier X4 | 01-28469H01 | Motorola |
| 1A2A6 | Diplexer | 01-20119J01 | Motorola |
| 1A2A7 | Mixer | 2523-BG | Sage Labs |

7.3.3 Checkout Equipment Power Supplies (1A3)

Power supplies to operate the V-C/O Equipment circuitry are contained in 1A3 drawer. These include commercial modular units supplying +9 vdc, -9 vdc, +3.5 vdc and circuitry to derive -3.5 vdc from the -9 vdc supply. The +3.5 vdc supply is actually operated at +5.2 vdc which permits further decoupling in the 1A1 drawer to +3.5 volts.

7.3.4 Vehicle Power Supply (1PS1)

A voltage of +28 vdc at 7 amperes for the AROD Vehicle-Borne Equipment is supplied by the 1PS1 drawer. The supply is a commercial unit (Lambda LM-F28) and is adjustable over a range of 24-32 volts to simulate various operational conditions during Vehicle Equipment Checkout.

7.3.5 Rack Cooling

A blower is installed at the bottom of the rack and is designed to keep the internal rack temperature rise to less than 15°C above ambient.

7.3.6 Size and Weight

Table 7-4 gives the size and weight of the V-C/O Equipment and various subassemblies.

TABLE 7-4. Equipment Size and Weights

| Assembly Name | Dimensions (inches) | | | Weight (lbs) |
|----------------------------|---------------------|-------|-------|--------------|
| | Height | Width | Depth | |
| V-C/O Rack, Complete | 60 | 21 | 28 | 470 |
| Control Drawer, 1A1 | 14 | 19 | 21 | 53 |
| R-F Translator Drawer, 1A2 | 10 $\frac{1}{2}$ | 19 | 22 | 55 |
| V-C/O Power Supplies | 5 $\frac{1}{4}$ | 19 | 12 | 32 |
| Vehicle Power Supply | 3 $\frac{1}{2}$ | 19 | 17 | |
| Electronic Counter | 5 $\frac{1}{4}$ | 19 | 16 | |
| Blower Assembly | 7 | 19 | 9 | |

7.4 VEHICLE CONTROL DRAWER, 1A1

7.4.1 Assembly Requirements

The Vehicle Control Drawer is divided into four basic sections. The left half of the drawer is simulator No. 1 and the right half, simulator No. 2. These halves are in turn divided laterally to separate rf and digital functions. Shielding is provided, in order to reduce crosstalk between simulators and to isolate the rf from the digital circuitry. Digital power wiring is separated from r-f power wiring by shields on the bottom of the drawer.

7.4.2 Design Approach

The fundamental design approach of the Vehicle Control Drawer followed designs, both mechanical and electrical, previously worked out for the AROD Transponder Station Equipment. The r-f modules are constructed in the 3-channel arrangement providing good rfi protection and allowing for convenient assembly. Digital modules are built on 6 x 6 inch motherboards and utilize to a great extent microharness modules developed for the Transponder Station.

7.4.3 Theory of Operation

7.4.3.1 Transponder Simulator Mode

Each of the transponder simulators is designed to work with three of the four Vehicle Equipment Receiver Channels. Simulator No. 1 on A, B, or C and Simulator No. 2 on channels B, C, or D. For simplicity, this discussion will be limited to simulator No. 1, but is applicable to simulator No. 2 if nomenclature and frequencies are changed.

The transmission is derived from a stable 12.8 MHz VCO located in module 1A1A7. The frequency may be set quite precisely with the ten-turn potentiometer (R1) on the drawer front panel. To obtain an output frequency of precisely 28.11875 MHz, a phase-locked loop is used, comprised of part of 1A1A5, 1A1A7, and 1A1A9. The operation is shown in the simplified block diagram, figure 7-6. The 12.8 MHz signal is doubled and mixed with the 28.11875 MHz to produce a difference output of 2.51875 MHz. This is shaped and divided, in 1A1A9, by 403 to provide a 6.25 kHz pulse output having approximately 20 - 80 percent symmetry. The 6.25 kHz output is multiplied by 64 and shaped to form a 400 kHz symmetrical square wave. The 12.8 MHz input to 1A1A9 is divided by 32 to provide another 400 kHz square wave. These two 400 kHz signals are compared in an "exclusive or" circuit which produces an 800 kHz output, the symmetry of which is dependent upon the phase relation of the two 400 kHz signals. The 800 kHz output is fed into an active loop filter which detects and amplifies the dc shift produced by the varying symmetry of the 800 kHz square wave. The output of the loop filter drives the 28.11875 MHz VCO, such that any change in dc output from zero volts produces a change in phase of the VCO, in turn driving the loop filter output back towards zero volts.

The phase-locked loop has the following characteristics:

| | |
|---------------------------|--------|
| Open loop gain | 15,750 |
| Loop filter dc gain | 23 |
| Noise Bandwidth (B_L) | 100 Hz |

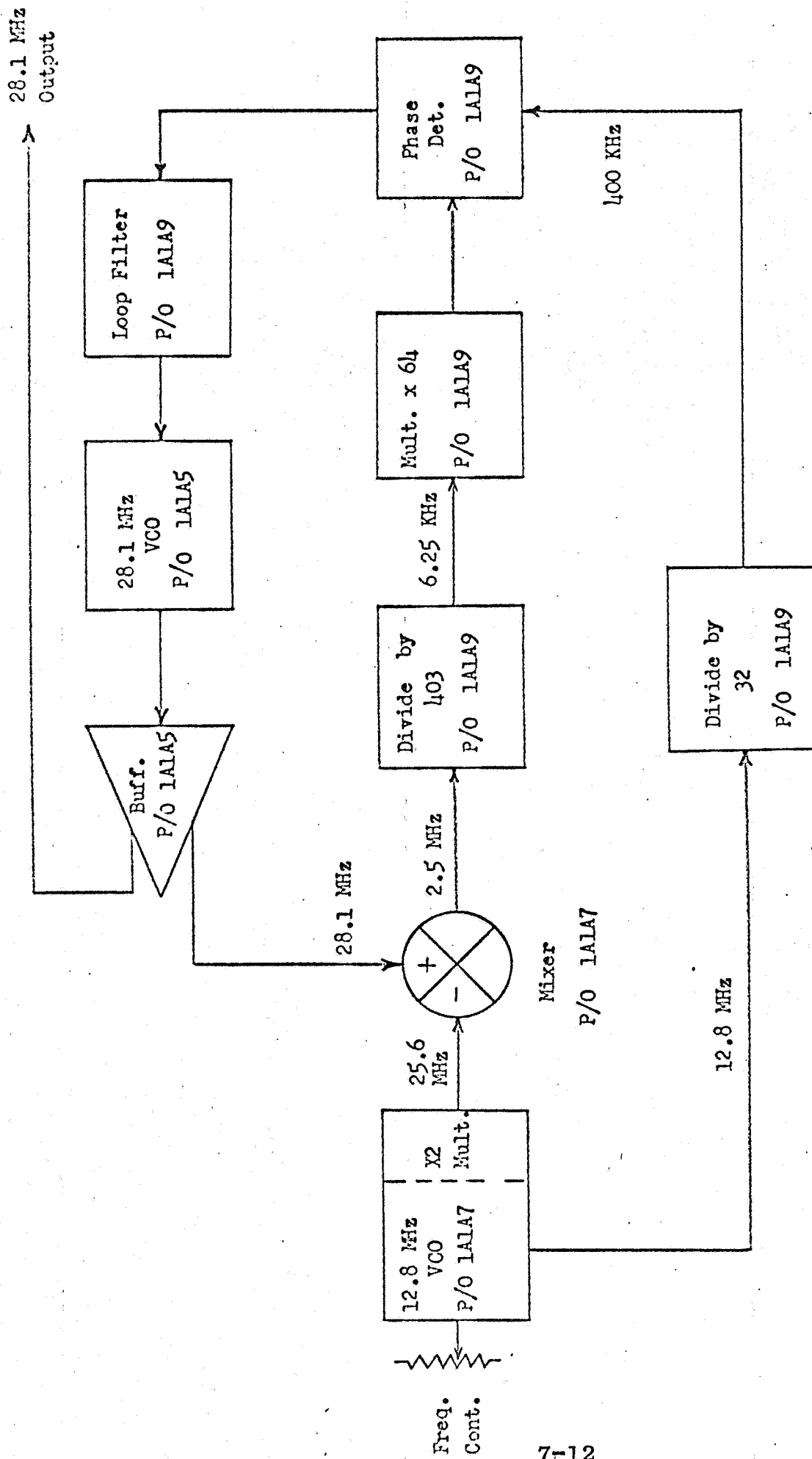


Figure 7-6. Transponder Simulator Synthesizer Loop, Simplified Block Diagram

In changing operation to Channel B, the channel VCO is changed to 28.125 MHz and the frequency divider is changed to 404. For Channel C, the VCO becomes 28.13125 and the divider 405. The proper VCO and divider ratio are selected by contacts on the CHANNEL SELECTOR, S53, on the front panel of 1A1 drawer. The output of the 1A1 drawer is then fed to the 1A2 drawer for a X64 multiplication resulting in:

| | |
|------------|---|
| Channel A: | $28.11875 \times 64 = 1799.6 \text{ MHz}$ |
| Channel B: | $28.125 \times 64 = 1800.0 \text{ MHz}$ |
| Channel C: | $28.13125 \times 64 = 1800.4 \text{ MHz}$ |
| Channel D: | $28.1375 \times 64 = 1800.8 \text{ MHz}$ |

Data for use in modulating the L-Band signal (accomplished in 1A2 drawer) are generated from the 12.8 MHz signal in the Code Control Unit, 1A1A11. Status of A_H and DRC, and site data, are generated in the Data Encoder, 1A1A12, and used to drive the code control unit to generate the complete Transponder Station modulation. Either "low-code" or "Track" mode may be selected by a front panel switch.

7.4.3.2 Translator, or Coherent, Mode

Since a major portion of the coherent mode circuitry is contained in the 1A2 drawer, a complete description of this mode is reserved for the discussion in paragraph 7.5.3.2.

The function of the 1A1 drawer in the coherent mode is to generate a subharmonic of the translation frequency of 414.4, 414.0, 413.6, or 413.2 MHz. This is done by utilizing the S-Band subharmonic, 34.59375 MHz, from the vehicle equipment. The 34.59375 MHz signal is mixed with the 28.1 MHz VCO signal to produce frequencies as follows:

| | |
|------------|--|
| Channel A: | $34.59375 - 28.11875 = 6.475 \text{ MHz}$ |
| Channel B: | $34.59375 - 28.125 = 6.46875 \text{ MHz}$ |
| Channel C: | $34.59375 - 28.13150 = 6.4625 \text{ MHz}$ |
| Channel D: | $34.59375 - 28.1375 = 6.45625 \text{ MHz}$ |

To generate these frequencies, the proper VCO and divider programming are selected by CHANNEL SELECTOR, S53. Transponder simulator No. 1 is used for channels A and B; whereas, simulator No. 2 is used for channels C and D. The code control units of 1A1 drawer are not used. However, an output of the 12.8 MHz reference VCO is fed to the Vehicle transmitter code control unit, along with site data from the code generators, to produce modulation on the Vehicle transmission which is coherent with the V-C/O 12.8 MHz VCO.

7.4.3.3 Code Control Units

A code control unit (1A1A11, 1A1A12) very similar in design to the Transponder Station code control unit is provided for each simulator. Each code control unit generates the transponder transmit Z code (c/o TT-Z and c/o TT- \bar{Z}) which is used to modulate the L-Band transmissions. It utilizes the 12.8 reference frequency to generate the H-code sequence and the L-code sequence. In addition, it accepts "S-Band Data" from the Data Encoder to produce the complete data signals. Provision is made to switch the output from $L \oplus D$ to $L \oplus H$ ($F_L \oplus F_L/2$) $\oplus D$ by use of a front panel switch, S48. The code control units are also capable of being preset by a delayed L_{127} pulse (RANGE, ADJUST & RESET).

7.4.3.4 S-Band Data Encoders

A data encoder (1A1A13, 1A1A14) is provided for each transponder simulator. It generates a 10-bit message format essentially the same as produced by the Transponder Station Control Logic. The generated message is transmitted at the rate of approximately 50 information bits per second, which corresponds to 1 bit per L-code period. The encoder utilizes L_{127} and L_{59} pulses from either the c/o code control unit or the Vehicle Code Control Unit, the selection of which being determined by the position of CHANNEL SELECTOR, S53. The sync portion of the coded output consists of 3 bits, having sub-bit logic levels of 111000.

The next 6 bits constitute the station ID and are programmable through the front panel switches (S29-34 for channel A-B-C, and S35-40 for Channel B-C-D). The last bit provides the status of A_H and DRC in accordance with the setting of control switches, S41, S42 (Channel A-B-C) and S43, S44 (Channel B-C-D).

Functional Description

The Station Control Logic Encoder Module, 69-24444G is used to generate the required S-band timing and data format. It also encodes the site ID code data for S-band transmission. The S-band data are transmitted to the vehicle in a 10-bit data format as shown in figure 7-7. The first 3 bits (6 sub-bits) are used as word sync, which is represented by the sub-bit pattern 111 000. Bits t_4 through t_9 are the site ID code, which are inserted by 6 toggle switches. The last bit, t_{10} , represents the station status. The significance of the two status sub-bits is given in table 7-5. The first sub-bit represents the status of $T-A_H$ and the second sub-bit represents that of Doppler-reverse-complete (T-DRC).

| | | | | | | | | | |
|-------|-------|-------|---------|-------|-------|-------|-------|-------|----------|
| t_1 | t_2 | t_3 | t_4 | t_5 | t_6 | t_7 | t_8 | t_9 | t_{10} |
| Sync | | | Site ID | | | | | | Status |

Figure 7-7. S-Band Data Format

TABLE 7-5. Station Status

| Status | | Bit 10 | |
|---------|-------|-------------|-------------|
| $T-A_H$ | T-DRC | 1st Sub-bit | 2nd Sub-bit |
| 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 |

The S-band data rate is approximately 50 bits per second. Each data bit is encoded into two sub-bits. A data bit ONE in the site ID code is encoded into a sub-bit ZERO followed by a sub-bit ONE, while a ZERO is encoded into a sub-bit pair of ONE - ZERO. The status data bit is uniquely encoded as described previously. The resulting transmission rate is approximately 100 sub-bits per second.

Implementation

The Encoder Module, 69-24444G, uses TL_{59} and TL_{127} from the transponder Code Control Logic as clock pulses. Gate G16 accepts and combines the two signals to form $TL_{59} + TL_{127}$, which is labeled as $2 CL_{SB}$. The output of G16 comes out of the module and is routed to an EX/OR (B6 of Figure 7-8), which selects either this clock or that of the checkout equipment clock, $C/O TL_{59} + C/O TL_{127}$ from gate G11, as determined by the gate control switch. Regardless of whichever input clock is selected, flip-flop FF6 (figure 7-8) divides the output pulses of the EX/OR by 2 to provide the Encoder Module with CL_{SB} and \overline{CL}_{SB} .

The 10-bit S-band data format is generated by a 10's counter, FF4, FF5, FF6 and FF7, in the Encoder Module. Flip-flops FF4, FF5, and FF6 are connected as a shift register with feedbacks gated through G13 and G14. FF7 is a simple binary toggle flip-flop. The 10 states of the counter and the corresponding T-pulses are given in table 7-6. Note that not all 10 states are explicitly used. Gates G21, G22, and G23 are arranged to pick out, respectively, the S-band T2, T3, and T9 pulses (no relation to the vehicle T-pulses). The S-band timing diagram is shown in figure 7-9.

The word sync pattern (111 000) is generated by selecting the second half of T2 with G12 and combining it with T3 at G11. G10 is used as an inverter to provide the proper phase for G20. The TRANSMIT ENABLE signal is grounded so that FF2 is set by T3

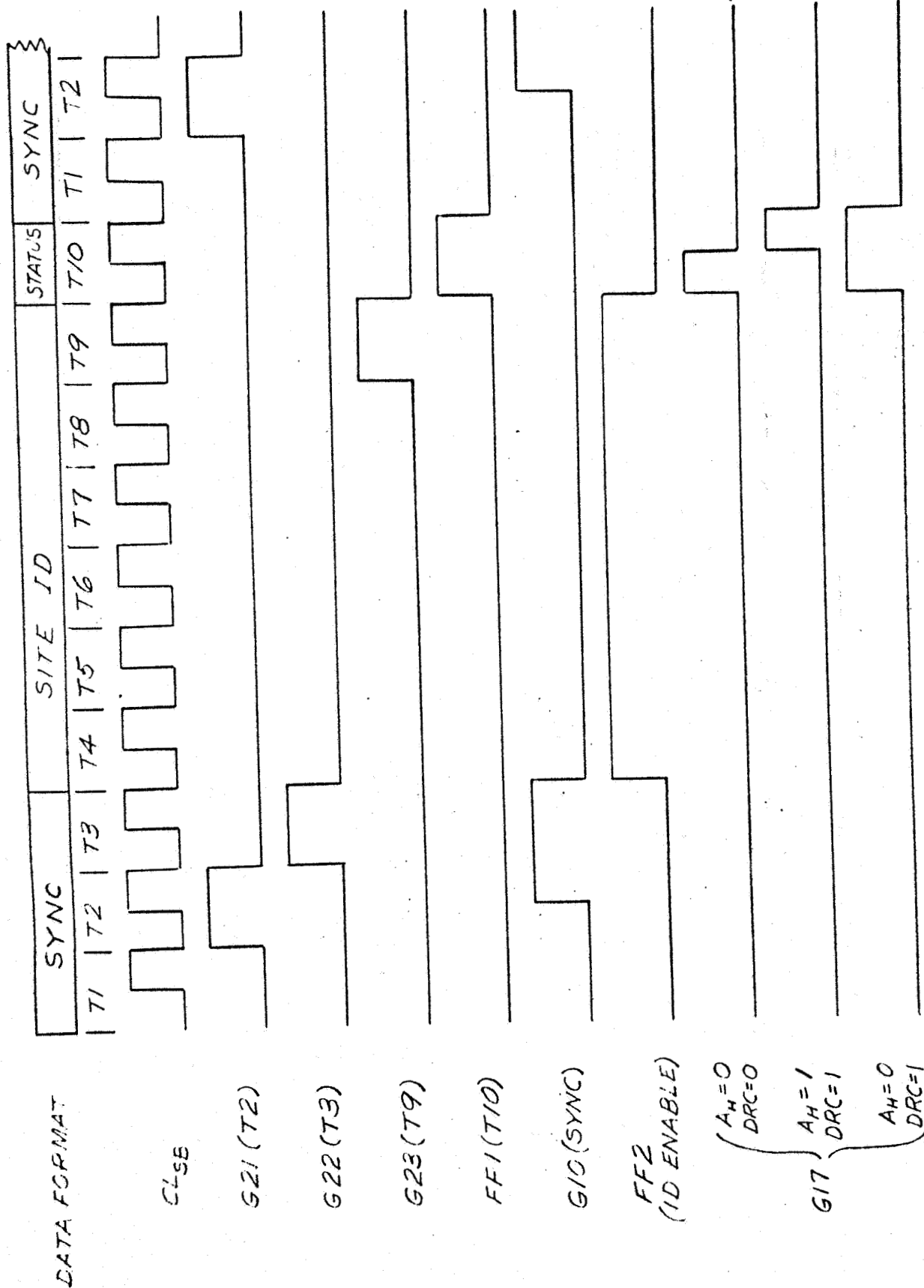


Figure 7-9. S-BAND TIMING DIAGRAM

TABLE 7-6. States of 10's Counter

| T-Pulse | FF4 | FF5 | FF6 | FF7 |
|---------|-----|-----|-----|-----|
| T1 | 1 | 0 | 0 | 0 |
| T2 | 1 | 1 | 0 | 0 |
| T3 | 1 | 1 | 1 | 0 |
| T4 | 0 | 1 | 1 | 0 |
| T5 | 0 | 0 | 1 | 0 |
| T6 | 1 | 0 | 0 | 1 |
| T7 | 1 | 1 | 0 | 1 |
| T8 | 1 | 1 | 1 | 1 |
| T9 | 0 | 1 | 1 | 0 |
| T10 | 0 | 0 | 1 | 1 |

through G4 and G5. The ZERO output of FF2 enables the site ID data to pass through either G18 or G19. FF2 is reset at T9, which also sets FF1 for one T-pulse period. The ZERO output of FF1 enables the station status data to pass through G17. The significance of the station status bit is given in table 7-5. The first sub-bit of T10 represents the status of T-A_H and the second sub-bit represents the complement of T-DRC. The sync, site ID data, and station status are combined by G10 to form a single serial output. The EX/OR, A1, is used as a data selection gate to accept either the output of G10 or external data, such as a new memory system. The actual data selection is determined by the state of FF3. If it is a ZERO, the output of G10 is transmitted to the vehicle, otherwise external data is transmitted. Whenever the LOAD MEMORY signal is a ONE, LOAD MEMORY is necessarily a ZERO, and FF3 is set by T10·CL_{SB} to select the external input data and to enable D1 to supply CL_{SB} clock pulses to the external data source. As long as the LOAD MEMORY signal remains a ONE, only external data are transmitted to the vehicle. However, as the LOAD MEMORY signal for the S-Band Manual Data Encoder is connected to Vcc, the external data mode of operation is effectively inhibited.

The S-band data format is always generated by the Encoder Module as long as Vcc and clock pulses are available. The site ID data and station status are inserted into the data format by the appropriate T-pulses. The site ID code is represented by 6 toggle switches, S1 through S6. These switches are arranged to either pick up the pertinent T-pulse or ground during the interval between T4 and T9. Since only T9 is available from the Encoder Module in this interval, a shift register (FF1 through FF5 of figure 7-8) is used to generate the required T-pulses. Gate G1 and expander G2 of figure 7-8 combine the output of the switches and furnish the Encoder Module with SITE ID DATA and SITE ID DATA.

The T-DRC and T-A_H signals are simulated by two toggle switches, S_{DRC} and S_{AH} respectively. Note that the ONE input to S_{AH} is ground while the ZERO input is Vcc. This is exactly opposite to the normal definition but is necessary so as to supply the Encoder Module with the correct interface signal. When the S_{AH} switch is at the ONE position, it implies that T-A_H is a ONE, but the actual output is low ($\overline{A_H}$). Gate G6 of the Encoder Module combines the S_{AH} switch output with CL_{SB}. The S_{DRC} output is combined with $\overline{CL_{SB}}$ by G9. The effect of gating the S_{AH} switch output with CL_{SB} and the S_{DRC} switch output with $\overline{CL_{SB}}$ is to encode the T-A_H signal into the first sub-bit and the T-S_{DRC} signal into the second sub-bit. Finally the output of G6 and G9 is gated through G17 by T10 (the ZERO output of FF1). The output of G17 is the complement of table 7-5.

The operation of the S-Band Manual Data Encoder is relatively simple. Assume that power and input clock pulses are properly connected. The Manual Data Encoder automatically generates the sync pattern and encodes the output of the site ID and station status switches. If the 6 site ID switches are all set at ZERO and the two station status switches are set at ONE, the S-band transmission data consist of 7 ONE-ZERO sub-bit pairs interlaced between the sync patterns.

A delay circuit, consisting of two discrete component one-shots, is also incorporated on the S-Band Encoder motherboard for providing a delayed TL₁₂₇ pulse (VTL₁₂₇) to the Vehicle Checkout (C/O) Code Control unit. The first-one-shot (O.S.#1) is triggered by the TL₁₂₇ input pulse and provides an output pulse, the width of which is variable from 0.2 - 13.3 milliseconds and controlled by an external potentiometer labeled TL₁₂₇ TIME DELAY CONTROL. The second one-shot (O.S. #2) is triggered by the trailing edge of the O.S. #1 output pulse and in turn provides an output pulse having a fixed width of 400 microseconds (nominal); this output pulse is further amplified by G10 and D3. A second input to D3 from the C/O CODE CONTROL switch is used as an enable for controlling the transmission of VTL₁₂₇ to the code control unit.

7.4.3.5 Time Pulse Generator

The Time Pulse Generator, 1A1A18, generates the waveforms necessary to effect a printout of the desired data word. The Vehicle Data Readout unit normally provides a serial stream of ten words of data to the telemetry equipment. The telemetry supplies pulses at the rate of 4 pps, this rate having a slightly larger period than required to encompass the entire data format between pulses. The pulses are referred to as "Reset TM" pulses. The Time Pulse Generator supplies the Reset TM pulses during test, by dividing down a 40 pps oscillator. In addition, it generates a "Print Command" pulse properly timed to the Reset TM pulse so that any one of the ten data readout words may be printed out on the HP-562A Digital Printer. The desired word is selected by the front panel switch, S58, WORD SELECT. The Time Pulse Generator also generates a "Reset RT" pulse, acutated by the front panel switch S59, which resets the Vehicle 5-minute timer.

7.4.3.6 Memory Program Generator

The Memory Program Generator consists of three modules, 1A1A15, 16, and 17, and although separated, they operate as a unit, tied to the front panel control switches S1-S28. The function is to load and/or read, the Vehicle magnetic core memory. The generator

is driven by an internal clock of approximately 800 Hz. In loading the memory, a series of 24 cycles is gated on, producing 12 bits of "Prime" data alternating with 12 bits of "Alternate" data. These 24 bits are programmable with switches S5 through S28. The series of 24 bits is repeated 5 more times, with coding switches reset each time, to load in the 6 prime and alternate station ID's and the 6 prime and alternate maximum ranges.

Twenty-four toggle switches are used to generate the load memory data where each switch represents a data bit. The 24 data bits are defined as a memory word, which consists of 6 bits each of prime and alternate site ID codes and their respective maximum range data. The data bit arrangement within a memory word is shown in Figure 7-10, where P_n and A_n , $n = 1, 2, \dots, 12$, represent respectively the n th bit of the prime and alternate site data. This is the exact position in which the prime and alternate site data are stored in the vehicle memory.

ONE MEMORY WORD

$P_1 A_1 P_2 A_2 P_3 A_3 P_4 A_4 P_5 A_5 P_6 A_6 P_7 A_7 P_8 A_8 P_9 A_9 P_{10} A_{10} P_{11} A_{11} P_{12} A_{12}$

Figure 7-10. Memory Word Data Format

In actual system operation, the vehicle memory is under the control of the System Control Logic. Memory data are serially read out, a complete word at a time, with P_1 first and A_{12} last. The System Control Logic separates the prime and alternate site data. The appropriate site ID data codes are transmitted to the transponder station in the same order in which they are read out of the memory. Since data are always read out in the same order as loaded into the vehicle memory, it is extremely important in setting up the 24 data switches that the low order bit of each group is loaded into the memory first. This is particularly true for the maximum range data. If they are loaded into the memory

in the opposite order, it is impossible for the vehicle System Control Logic to obtain meaningful results from the maximum range data comparison operation.

The Memory Program Generator is built on 3 motherboards, excluding the indicator light and switches which are located on the front control panel. The logic diagram is shown in Figure 7-11.

Load Memory

The Memory Program Generator provides two modes of operation, READ or LOAD, according to the setting of the READ/LOAD switch. This section describes the LOAD memory logic as given in Figure 7-11. The READ operation is described in the Read Memory section.

The basic input clock is labeled 2CL. It may be either internal or external. For convenience, an oscillator, D1 and D2, is built into the Generator which may be used as the 2CL clock source. Flip-flop FF5 divides the 2CL clock by 2 to furnish the CL and $\overline{\text{CL}}$ pulses for internal operation.

Assume that the READ/LOAD switch is in the LOAD position and the operation switch is OFF. The 24 data switches are properly set to provide the required data for the first word to be loaded into the memory. As long as the operation switch is in the OFF position, the Generator is inoperative due to the fact that the output of G2 is a ONE (high level). When the operation switch is changed from the OFF to the ON position, the following events occur:

1. The output of G1 immediately becomes a ONE which forces a ZERO at the output of G2 to enable the Generator to operate according to the setting of the READ/LOAD switch.
2. Gate G13 combines the output of G2 and LOAD MEMORY to put a ONE on the LOAD MEMORY output line for the vehicle memory control logic.

3. G19 detects the different states in FF1 and FF2, and sends a one-shot pulse to preset the vehicle memory word counter to the last word position. Flip-flop FF21 is set by the PRESET pulse to turn on a lamp on the front panel, which indicates that the Generator is in the load memory mode.

After the Memory Program Generator completes the above housekeeping routines, it is ready for the actual execution of the load memory operation.

The load memory data are provided by the 24 data switches. These switches are labeled P_1 through P_{12} and A_1 through A_{12} as shown in Figure 7-11. Switches P_1 through P_6 are used to generate the prime site ID code and P_7 through P_{12} its maximum range data. P_1 and P_7 represent the low order bits, 2^0 , of their respective groups while P_6 and P_{12} the high order bits, 2^5 . The A_n switches are similarly divided to generate the required data for the alternate site. These data are serially loaded into the vehicle memory in a fixed word format, as shown in Figure 7-10. The prime and alternate site data are interlaced in such a manner that the prime site data are always located in the odd bit positions and the alternate site data in the even bit positions counting from left to right. For a given memory word, P_1 enters the vehicle memory first and A_{12} last; i.e., low order bit first. For most practical purposes, if the site ID codes enter the vehicle memory in the opposite order, it is possible to set the site ID switch bank in the transponder station accordingly so that it responds to the appropriate set of 4 site ID codes stored in the vehicle memory. However, the maximum range data must enter and leave the vehicle memory low order bit first, otherwise the maximum range data comparison operation performed by the vehicle system control logic is meaningless.

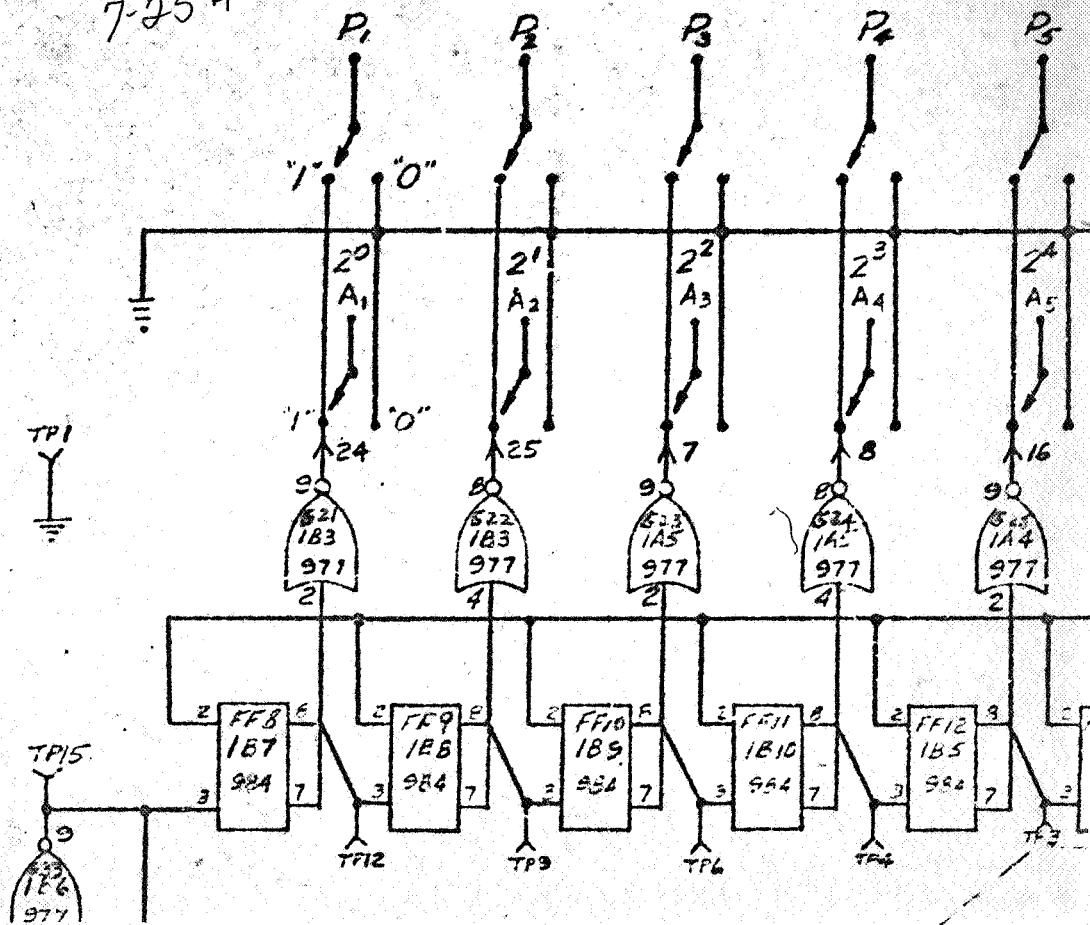
The actual load memory operation cycle is initiated by the START/ADVANCE push button switch. The output of the switch is

NOTE: P₁ THRU P₆, PRIME STATION SITE ID
A = ALTERNATE.

FOLDOUT FRAME

FOLD

7-25 A

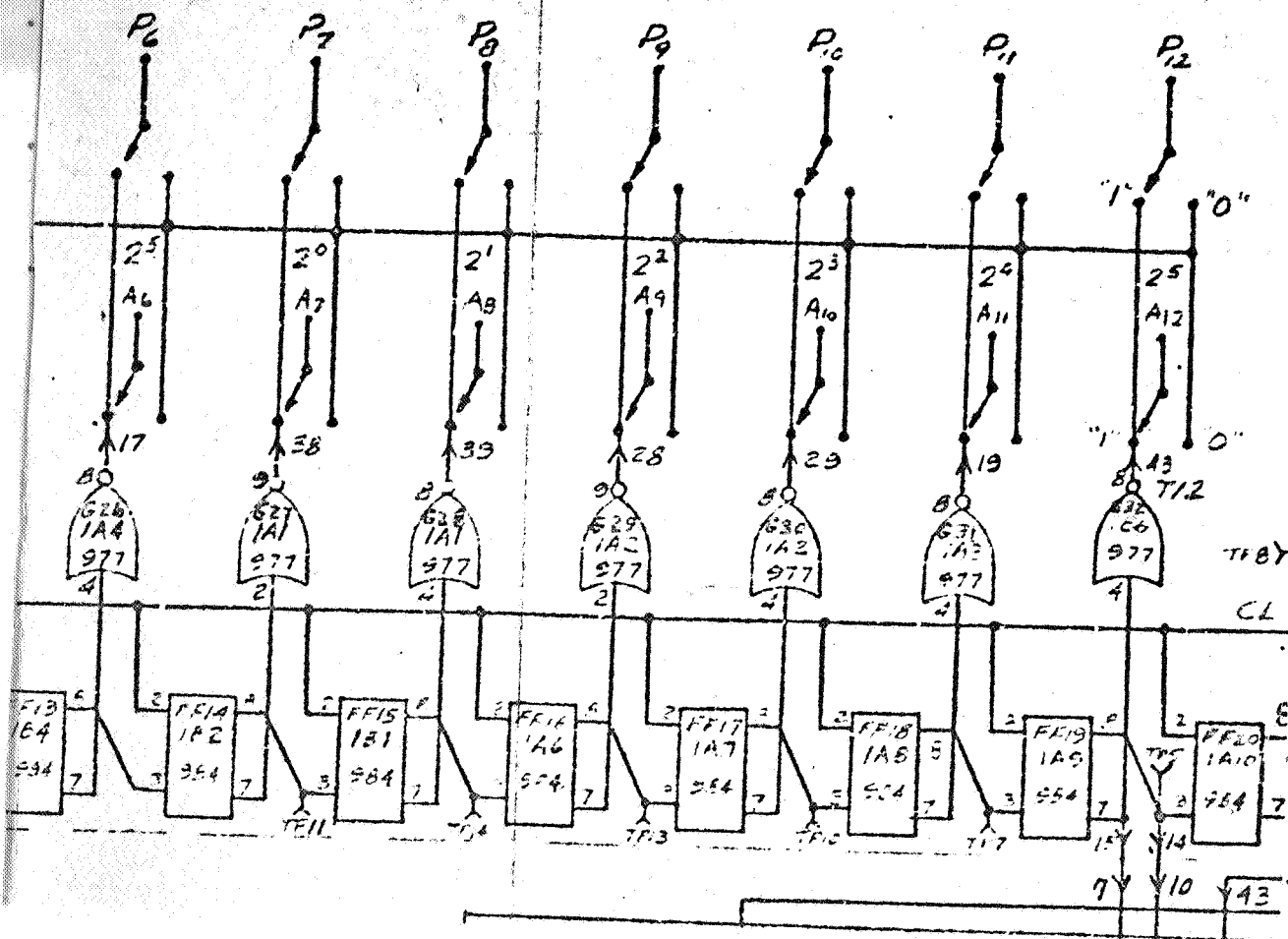


SWITCHES, P_7 THRU P_2 = RANGE

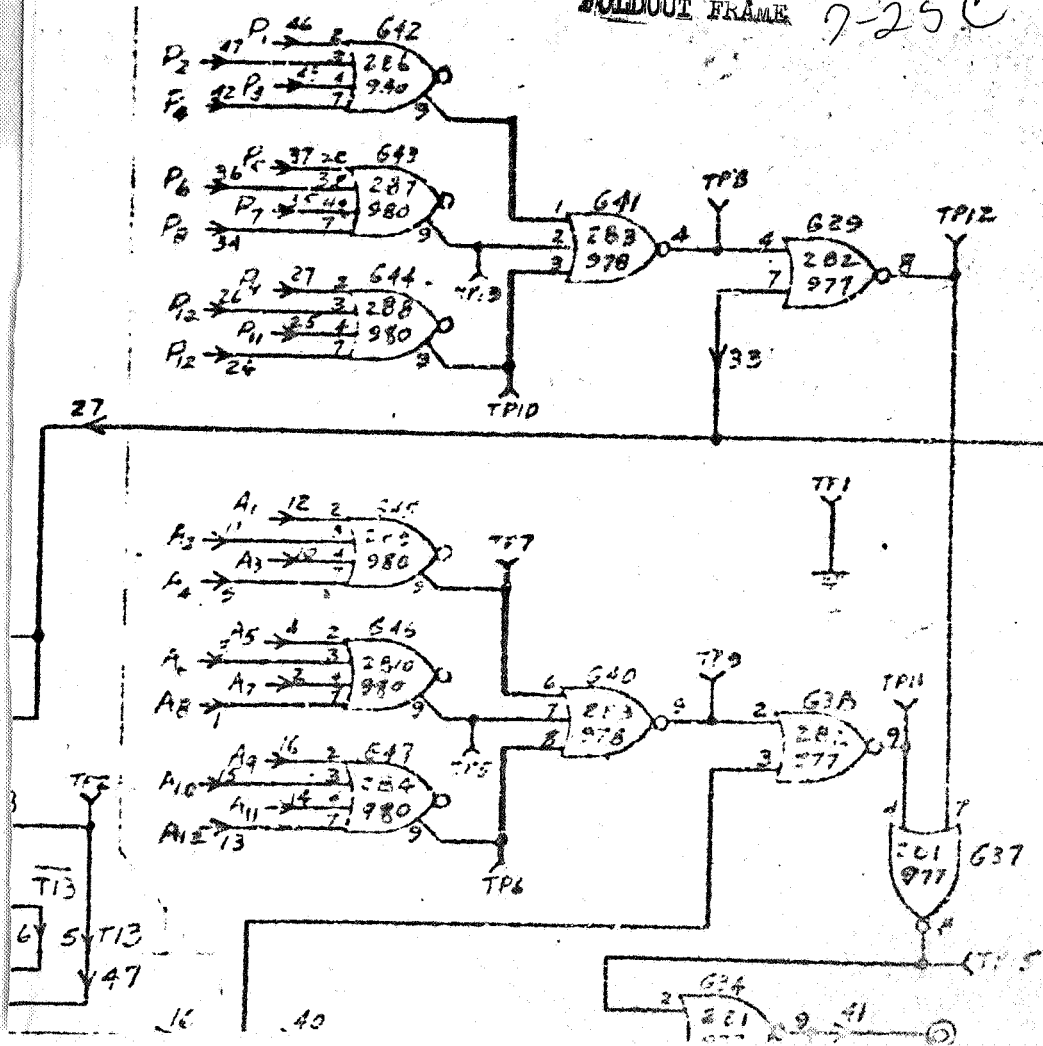
FOLDOUT FRAME

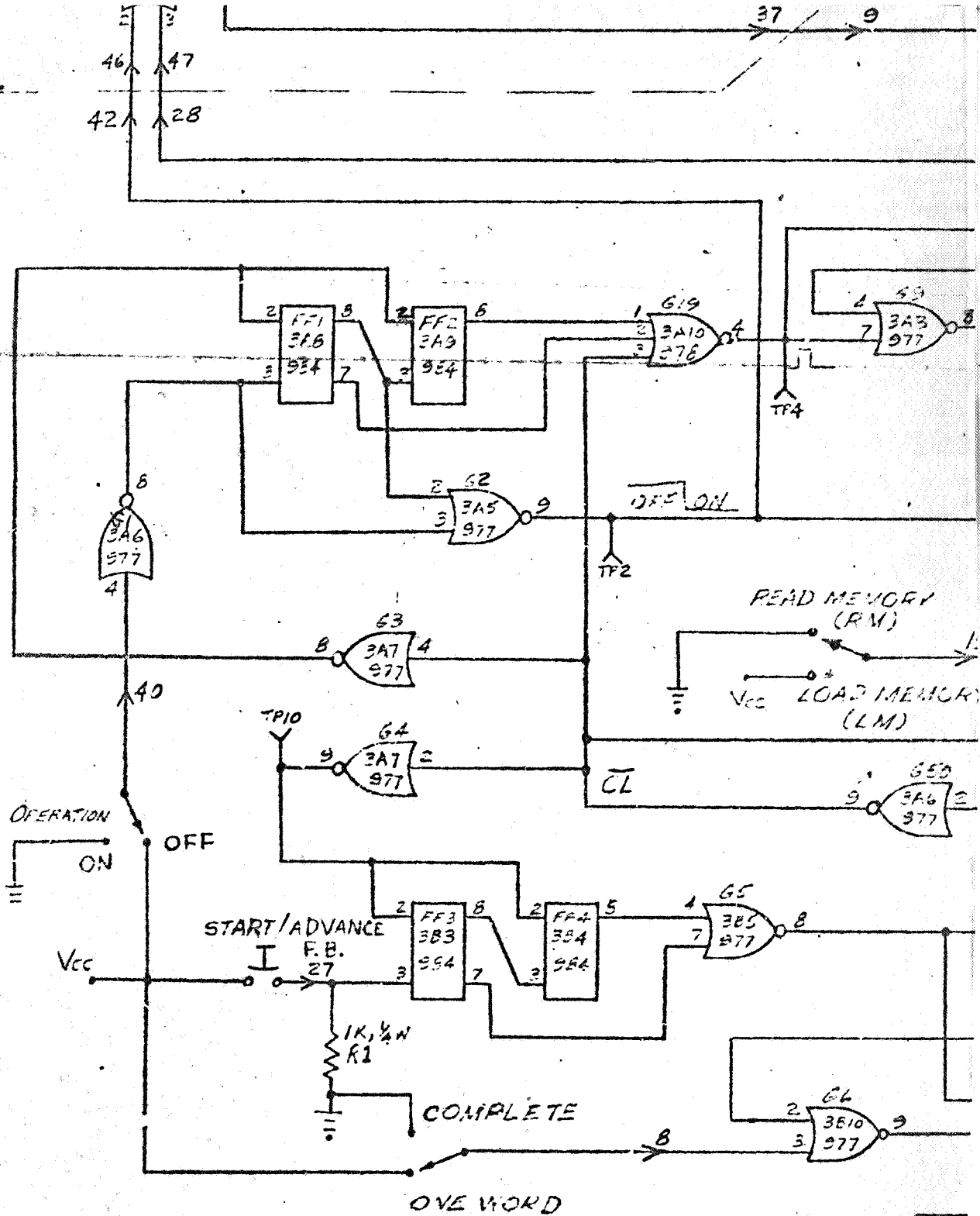
7-25 B

OUT FRAME



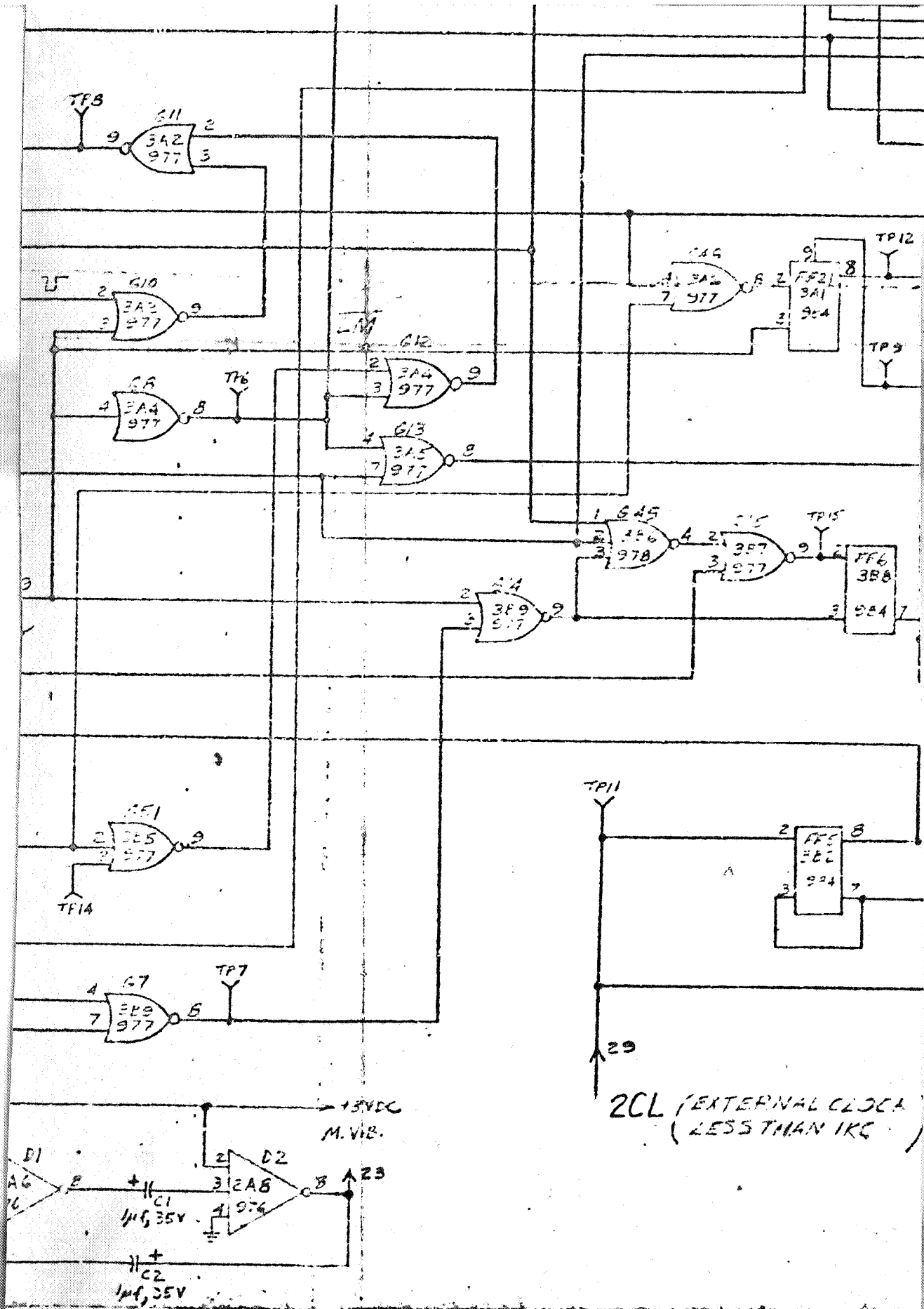
FOLDOUT FRAME 7-25C



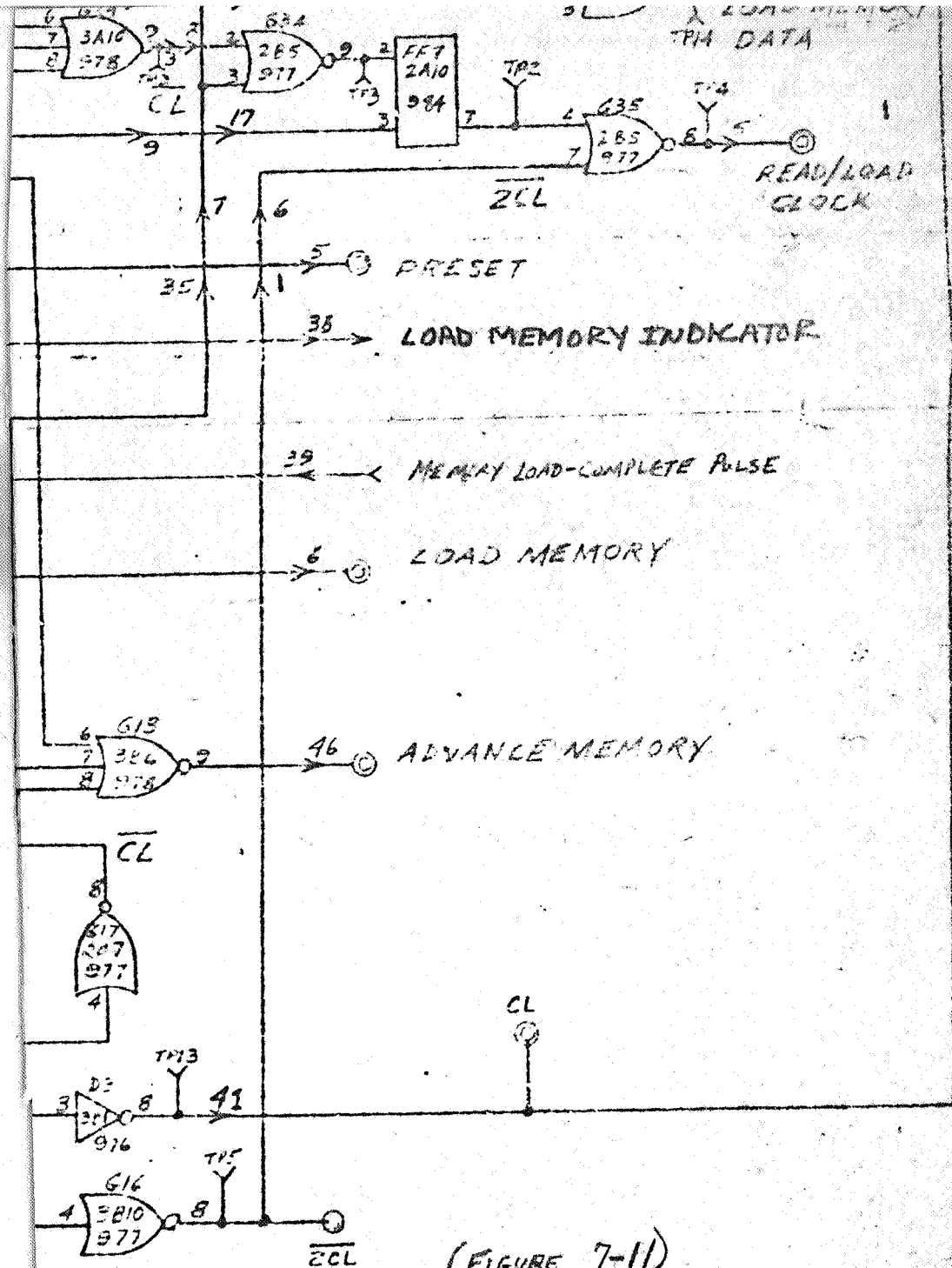


FOLDOUT FRAME

7-25 D



2CL (EXTERNAL CLOCK)
(LESS THAN 1KC)



(FIGURE 7-11)
 69-24634 G
 MEMORY PROGRAM
 GENERATOR

W-15-6

LINE 45

X 2-7-66

FOLDOUT FRAME

7-25 F

7-25

PRECEDING PAGE BLANK NOT FILMED.

shifted into FF3 and FF4 by the CL pulses to synchronize the switch output with the internal timing pulses as shown in Figure 7-12, and to eliminate contact bounce. The output of G5 is a one-shot pulse which starts the T-pulse generator, FF8 through FF20. As a ONE is shifted into FF8, gate G21 applies a positive pulse, T1, which is one CL period wide, to the ONE side of both data switches P_1 and A_1 . The other T-pulses are similarly applied to the corresponding data switches. The output of all prime site data switches are combined together by G42, G43, G44, and G41 to form a single output. The output of the alternate site data switches are similarly combined by G45, G46, G47, and G40. The prime site data are controlled by the CL pulses at G39 and the alternate site data by the \overline{CL} pulses at G38. The prime and alternate site data are finally combined together at G37 before they are loaded into the vehicle memory through G36. The effect of gating the prime site data with CL and the alternate site data with \overline{CL} is to divide each T-pulse into two halves with the prime site data occurring in the first half and the alternate site data during the second half. Therefore, two data bits are loaded into the vehicle memory during each T-pulse period.

As the LOAD MEMORY DATA emerges from G36, the vehicle memory control logic is provided with exactly 24 READ/LOAD clock pulses by G35. These 24 pulses are synchronized with the load memory data by FF7, which is set by the start pulse at the same time as FF8 of the T-pulse generator. After the last data bit, A_{12} , of a memory word is loaded into the vehicle memory, FF7 is reset at T12. The memory control logic automatically advances the word counter to the next word position. Additional words may be loaded into the memory by repeating the load memory procedure described above. When the vehicle memory is completely loaded, it sends a LOAD MEMORY COMPLETE signal back to the Generator to reset FF21, which turns off the load memory indicator light. Although the indicator light is turned off after the vehicle memory is completely loaded, the Memory Program Generator remains in the LOAD memory mode. Until the READ/LOAD switch is manually changed to READ, the

START/ADVANCE pushbutton switch always sets FF21 to keep the load memory indicator light on and loads data into the vehicle memory. After the vehicle memory is completely loaded, the OPERATION switch must be returned to the OFF position so as to prevent accidental loading of unwanted data into the memory.

Read Memory

The Memory Program Generator may be used to read data out of the vehicle memory. The READ operation is intended primarily as a means to verify the correctness of the data loaded into the vehicle memory. There are two options in which data may be read out of the vehicle memory, depending on the position of the COMPLETE/ONE WORD switch. If the switch is in the COMPLETE position, the Memory Program Generator supplies the vehicle memory with the required READ clock pulses and an advance memory signal to completely recycle the vehicle memory. If the switch is set at the ONE WORD position, only the selected memory word is repeatedly read out. The desired word is selected manually with the START/ADVANCE P.B. switch.

It is not premissible to change the position of the READ/LOAD switch unless the OPERATION switch is in the OFF position. When the READ/LOAD switch is in the READ position, the output of G8 inhibits the LOAD MEMORY DATA at G36 and also forces the LOAD MEMORY signal, output of G13, to become a ZERO. The actual READ memory operation starts with the OPERATION switch. As the switch position is changed from OFF to ON, G19 generates a one-shot pulse as described in the LOAD MEMORY section. This one-shot pulse is used to preset the vehicle memory word counter to the last word position and is gated through G9, G10, G11, and G33 to start the T-pulse generator and to set flip-flop FF7. Gate G35 is enabled by the reset output of FF7 to supply the vehicle memory with 2CL READ/LOAD clock pulse. As the T-pulse generator counts to T12, FF7 is reset to inhibit the READ/LOAD clock pulses at G35, so that only twenty-four (24) 2CL pulses are supplied to the vehicle memory per READ cycle. If the COMPLETE/ONE WORD switch is set at complete, $\overline{T12}$ is gated through G6, G7, G14, and

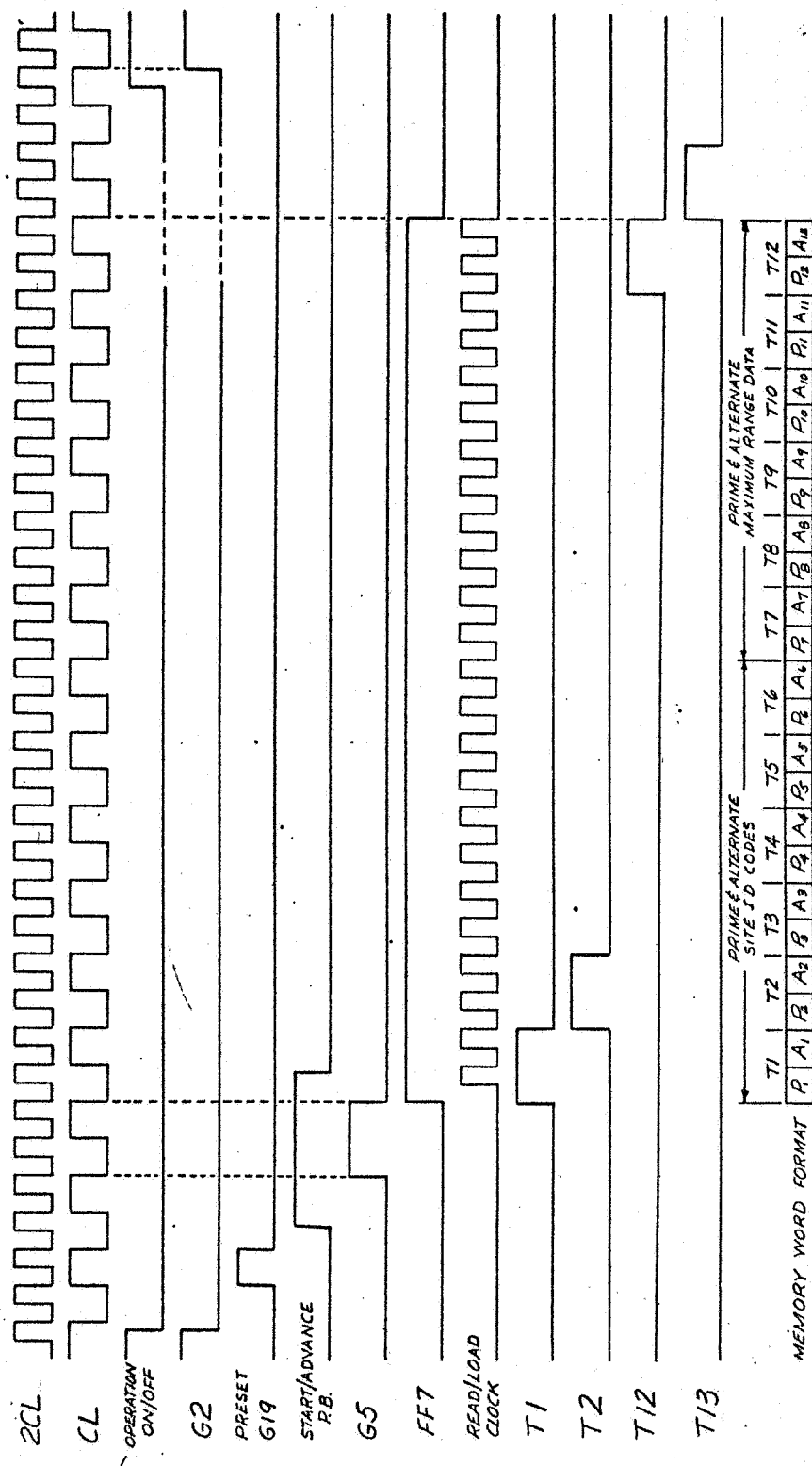


Figure 7-12. Load Memory Timing Diagram

G49 to set flip-flop FF6 for one CL pulse period which enables G18 to clock T13 to advance the vehicle memory word counter to the next word position. T13 resets FF6 and at the same time it is recirculated through G9 to restart the T-pulse generator and also sets FF7 to read the next word. The READ cycle is repeated every 13CL pulses until it is stopped by the OPERATION switch.

If the COMPLETE/ONE WORD switch is in the ONE WORD position, the automatic advance memory feature is removed by inhibiting T12 at G6. The same word is repeatedly read out. The desired word is selected with the START/ADVANCE P.B. switch. When this switch is actuated, G5 generates a one-shot pulse to set FF6, which allows only the next T13 to pass through G18 to advance the vehicle memory word counter. Therefore, the desired word can always be located by the use of the START/ADVANCE P.B. switch.

7.4.3.7 Lamp Drivers

The Vehicle Control drawer contains two identical lamp driver modules, 1A1A19 and 1A1A20. Each module is designed to drive 16 lamps, 8 with logical "1" input and 8 with logical "0" input. The circuit makes use of half-wave rectified alternating current as a lamp source. In addition to the saving in d-c power supplies, this arrangement permits the use of a simple, self-quenching silicon controlled rectifier driver. The circuits are designed to be positively "ON" or "OFF" as required with an input of 0 to 0.25 vdc and to switch at a voltage greater than 0.75 vdc. To provide isolation for the Vehicle Equipment circuitry, a 5600 ohm resistor is provided in each status line. Standard logic levels are received for V_4 state, A_L and A_H . Inverted logic levels are received for the V_0 , V_1 , V_2 , and V_3 states.

7.4.3.8 Variogon Phase Shifter

The Variogon Phase Shifter is a proprietary design of the Nilsen Company. It utilizes their special capacitive resolver producing a smooth 360 degree phase shift to the 12.8 MHz input for each revolution of the resolver dial. Tuned amplifiers are provided to

give the unit an overall gain of essentially zero dB, and to limit harmonic and spurious content in the output to an extremely low level.

7.4.3.9 VHF Demodulator

A simplified block diagram of the VHF Demodulator is shown in Figure 7-13. The VHF Demodulator utilizes a passive discriminator followed by an integrator to recover the 18.75 kHz subcarrier from the 138 MHz carrier. The discriminator is wide bandwidth (1 MHz) and fairly low in sensitivity, requiring an input of about +20 dBm from the 1A2 drawer. The 18.75 kHz output is amplified and fed into a balanced demodulator.

An 18.75 kHz input from the AROD Vehicle is delayed such that it is precisely 180 degrees out-of-phase with the 18.75 kHz subcarrier and shaped into a sine wave. (Since the latter was derived from the former in the Vehicle equipment, there is no problem of synchronization.) This signal is also fed into the balanced demodulator. The output is a three-level logic signal, which, when amplified and filtered, can be compared to the original sub-bit data.

7.5 R-F TRANSLATOR DRAWER, 1A2

7.5.1 Assembly Requirements

The assembly provides a calibrated output at 1800 MHz at levels down to -140 or -150 dBm. This requires exceptionally good shielding, especially from the input of the calibrated attenuator to the output terminal of the drawer.

7.5.2 Design Approach

The drawer is divided vertically by a horizontal plate. D-C, 60 Hz ac, and 138 MHz VHF signals are contained in the bottom section, with the dc and 60 Hz AC partitioned off from the 138 MHz. The upper compartment contains all S-Band signals as well as the subharmonics used to generate them. A separate compartment is provided for the 100 dB calibrated attenuator and diplexer.

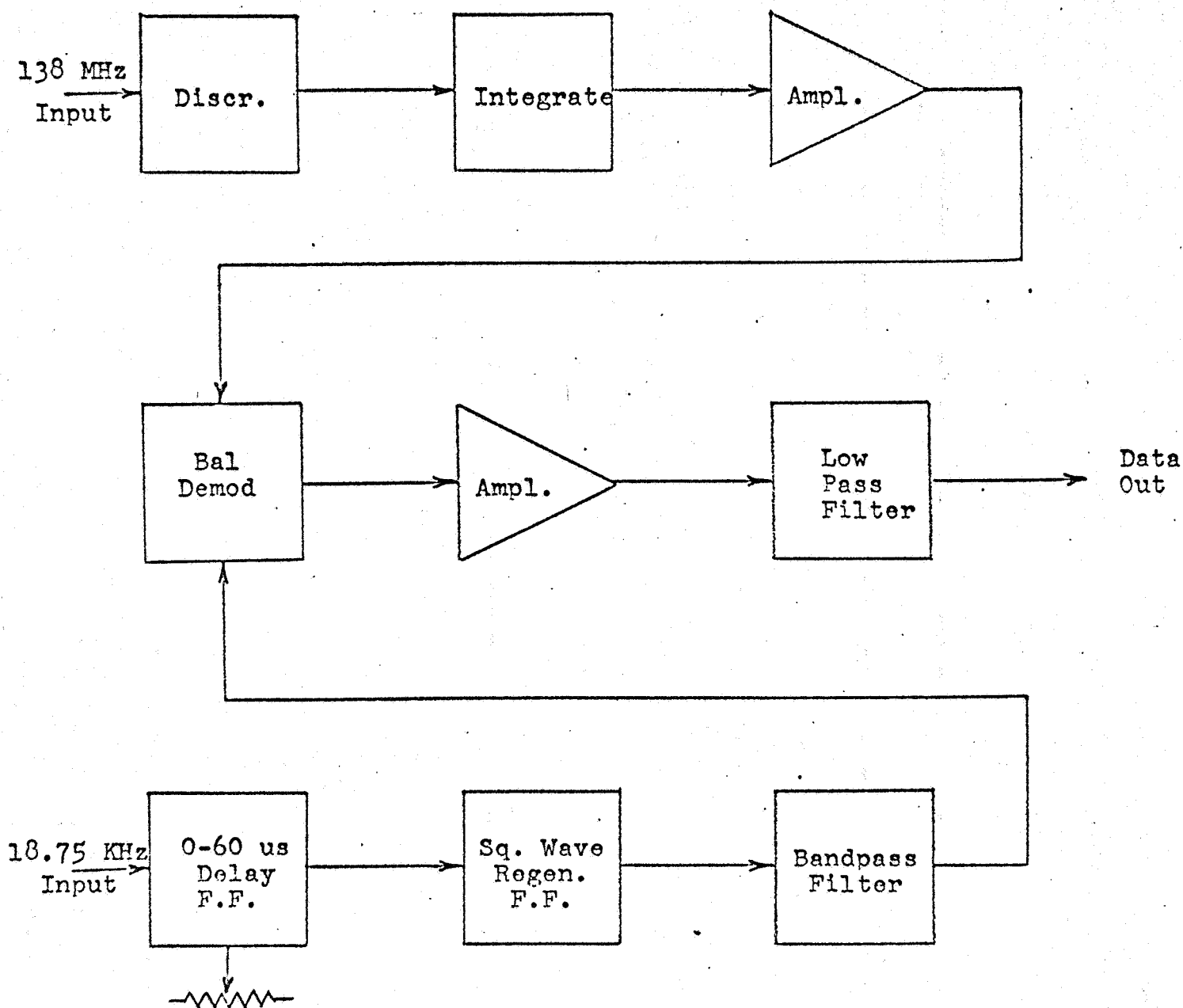


Figure 7-13. VHF Demodulator, Simplified Block Diagram

All surfaces are gold plated and all panel-mating surfaces have wide flanges with double gasketing of "Metex".

7.5.3 Theory of Operation

7.5.3.1 Transponder Simulator Mode

A simplified block diagram, showing only those components used in this mode is given in Figure 7-14. An input frequency of 28.11875, 28.125, or 28.13125 MHz, depending upon the channel of operation, is fed to J5 and a frequency of 28.125, 28.13125, or 28.1375 MHz to J6.

Modules A1 and A2 are identical. Each contains an X2 and an X4 multiplier, followed by a biphase modulator and a final X2 multiplier. The 450 MHz output is fed to a passive, "strip-line" X4 multiplier which utilizes a step-recovery diode. The outputs of the two X4 multipliers are fed through fixed attenuators and adjustable attenuators permitting individual channel level-set adjustments from the front panel of the drawer. The two simulator outputs are combined in AT9 and fed into the calibrated attenuator at a level at approximately -40 dBm. The output at J24 is taken through the diplexer A6. In operation, the Vehicle output at 2214 MHz is present at the other output of the diplexer, but is not used in this mode. Either simulator may be turned ON or OFF by a switch on the front panel of the 1A1 drawer. This operation controls the application of +9 volts to the X16 multiplier.

7.5.3.2 Translator or Coherent Mode

A simplified block diagram of 1A2 components used in the coherent mode is given in figure 7-15. Transmission is possible on only one channel at a time, depending entirely upon the frequency of the 6.4 MHz signal input at J7 (from 1A1 drawer).

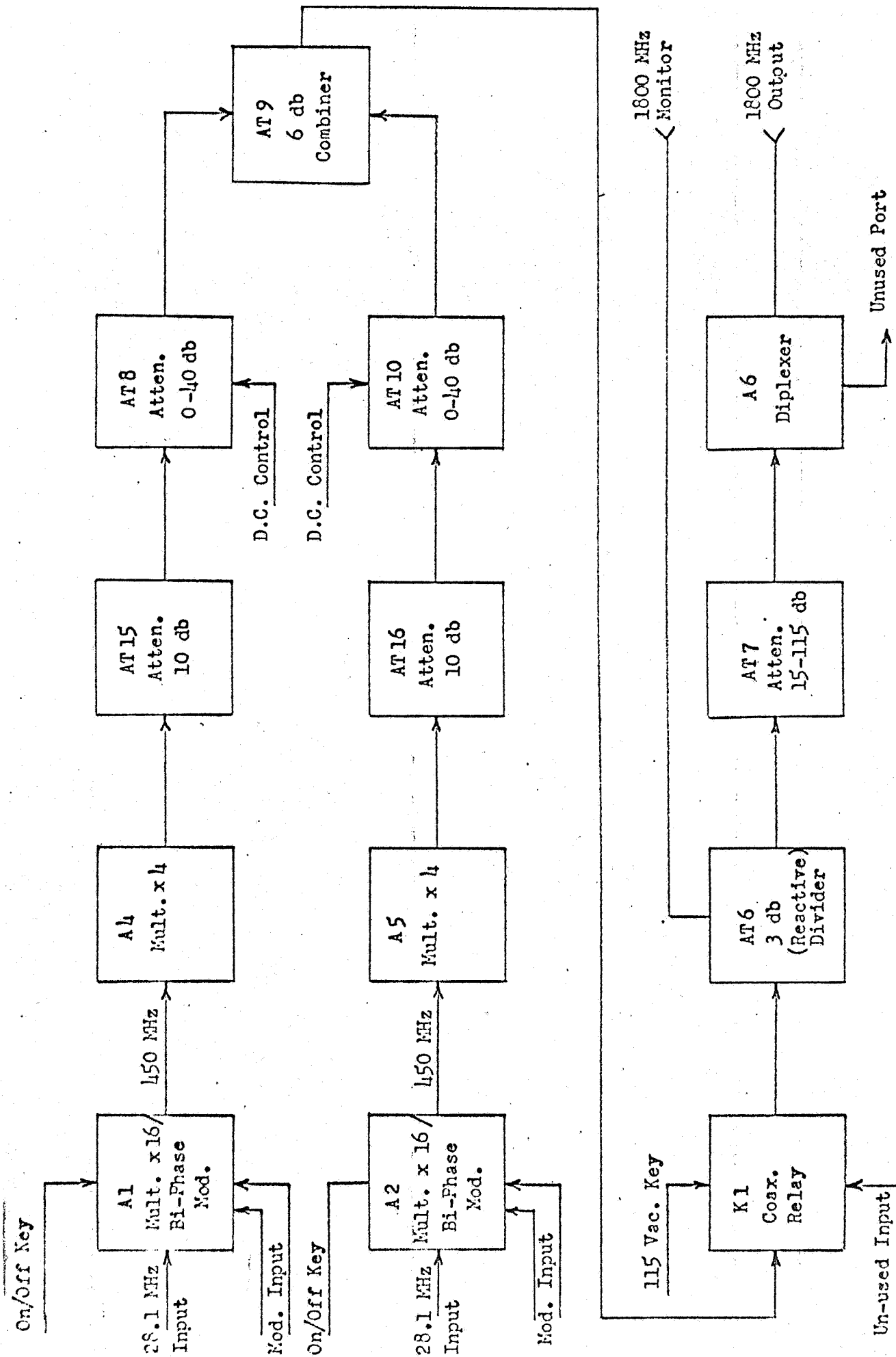
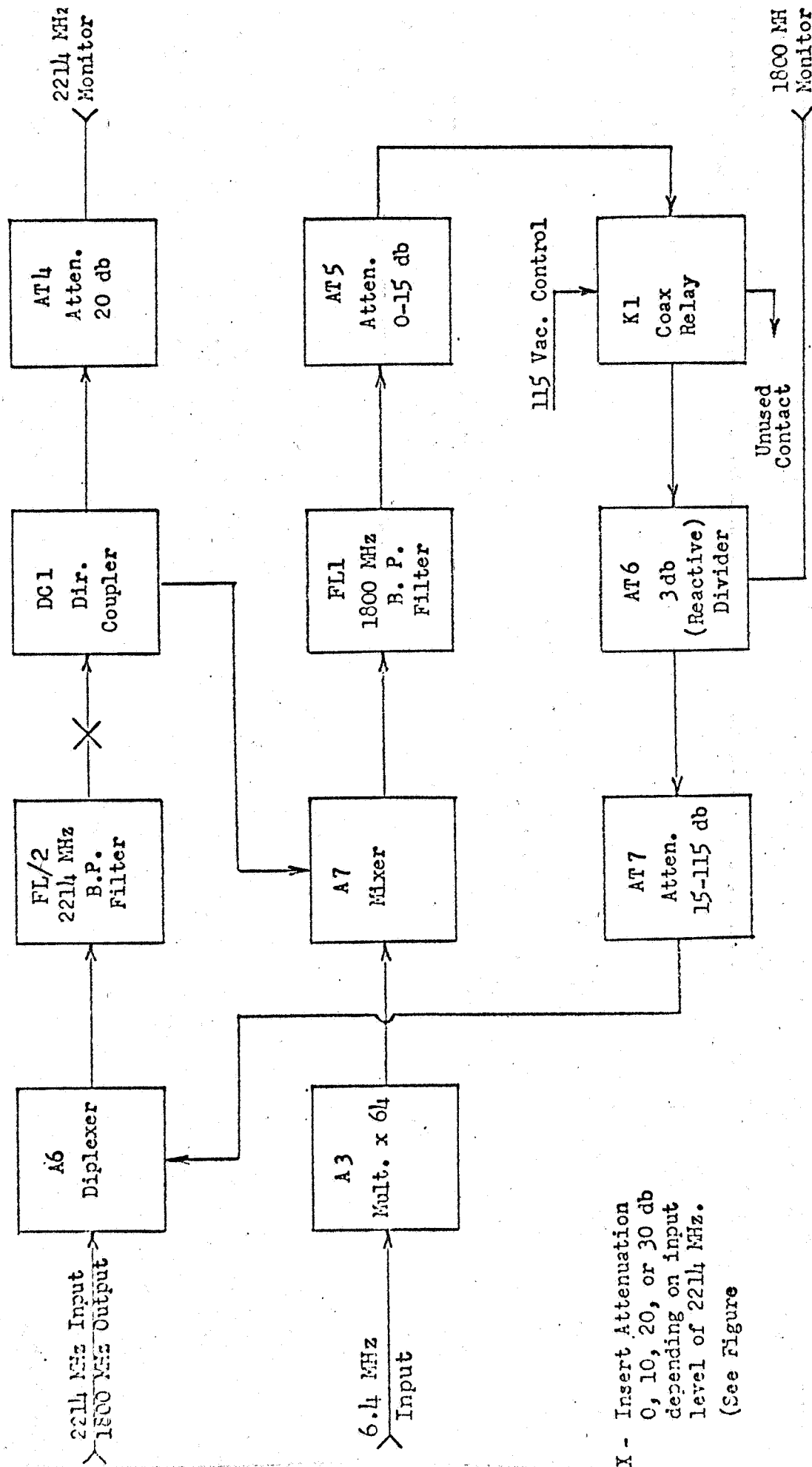


Figure 7-14. Transponder Simulator Mode, Simplified Block Diagram



X - Insert Attenuation
0, 10, 20, or 30 db
depending on input
level of 2214 MHz.
(See Figure

Figure 7-15. Coherent Mode, Simplified Block Diagram

This signal (defined in paragraph 7.4.3.2) is multiplied up to 414 MHz in A3 and mixed in A7 with a reduced amplitude, 2214 MHz signal from the Vehicle Tracking Transmitter. The difference frequency output of the mixer, 1800 MHz, is then amplitude-controlled and fed out through the diplexer, A6, to form the Vehicle receiver signal. In this configuration, the master frequency control is the V-C/O 12.8 MHz VCO. Any error, or offset, in frequency appears as Doppler, and is multiplied up along with the signal and appears as the correct algebraically multiplied Doppler on the 2214 MHz signal. The V-C/O 12.8 MHz VCO also controls the Vehicle Transmitter Code Control in this mode, which in turn provides the S-Band modulation. This results in the correct Doppler on the modulation as well. As the Doppler consideration may be difficult to understand, consider the following diagram, Figure 7-16.

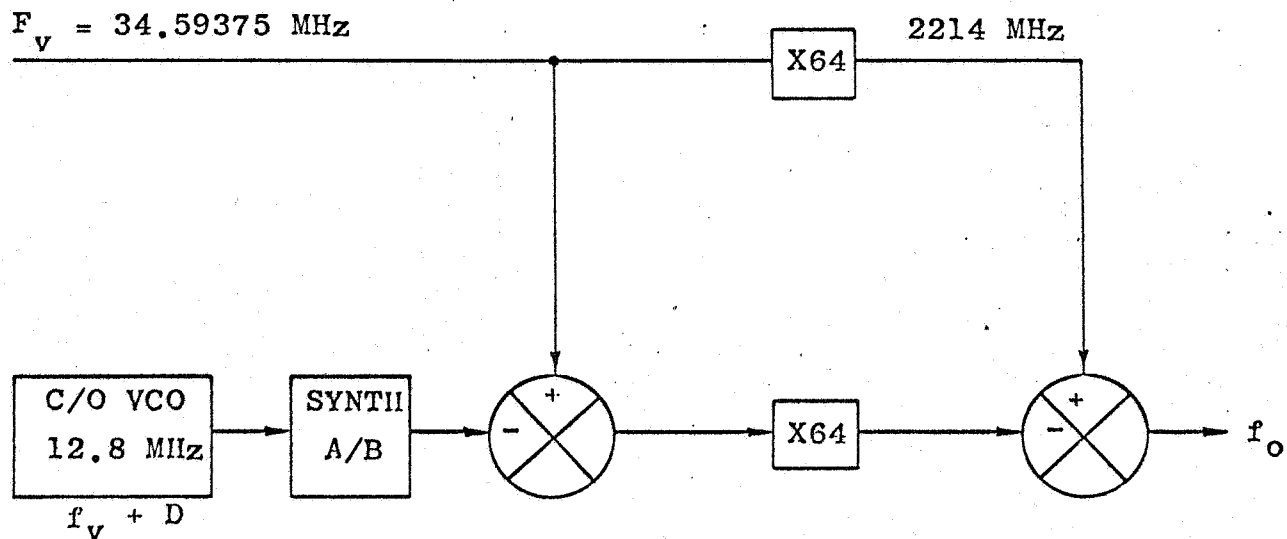


Figure 7-16. Doppler Consideration

F_v is from the Vehicle frequency synthesizer and is assumed constant. f_v is the V-C/O VCO assumed to vary in phase and frequency with respect to the Vehicle 12.8 MHz VCO. D is the Doppler offset, which is actually the difference in the Vehicle and V-C/O 12.8 MHz signals.

The 2214 MHz signal is then $64 F_v$. The output frequency f_o is:

$$\begin{aligned} f_o &= 64 F_v - 64 \left[F_v - (f_v + D) \frac{A}{B} \right] \\ &= 64 F_v - 64 F_v + 64 (f_v + D) \frac{A}{B} \\ &= 64 \cdot \frac{A}{B} (f_v + D) \end{aligned}$$

which shows the Doppler to be multiplied by precisely the same factor as the V-C/O VCO.

If the V-C/O VCO is replaced with the Vehicle 12.8 MHz VCO, which can be done by proper patching on the front panel of the 1A1 drawer, the 1800 MHz signal will have no Doppler. Further, it will have a phase relationship to the 2214 MHz signal of a small, fixed magnitude determined solely by the V-C/O Equipment delay.

7.5.3.3 VHF Circuitry

The VHF circuitry consists of attenuators and provides a monitor point for the Vehicle Station Control Transmitter. A block diagram showing this portion of the 1A2 drawer is given in Figure 7-17.

7-6. POWER SUPPLY, V-C/O (1A3)

The 1A3 drawer contains three commercial, modular power supplies, +9 vdc, -9 vdc, and +3.5 vdc, which supply power to the V-C/O circuitry. A -3.6 vdc source is derived from the -9 v supply by a zener diode. An additional +3.6 vdc source, derived from the +9 v supply is generated and used to reset the Vehicle System Control Logic. Application of this voltage is effected by depressing "ACQUISITION" switch, S2, on the front panel of 1A3. Plus 5 volt reference voltages for the digital printer are obtained from a voltage divider across the +9 volt supply.

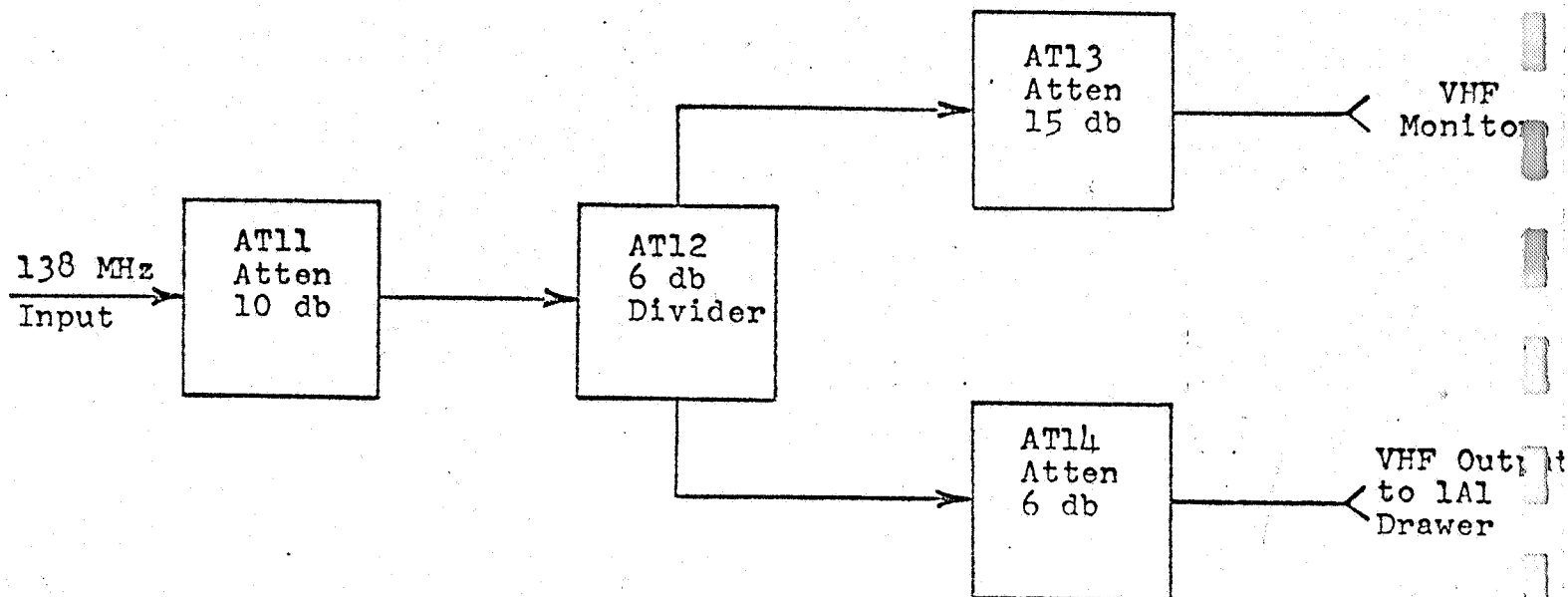


Figure 7-17. VHF Circuitry, Simplified Block Diagram

Separate fusing for the three supplies is not necessary since the supplies have adequate built-in short protection for the load side. The fuse, F1, offers sufficient protection for a short in the AC wiring. For a schematic diagram of the 1A3 drawer, refer to Drawing No. 69-28087J.

SECTION VIII

8. TRANSPONDER CHECKOUT EQUIPMENT

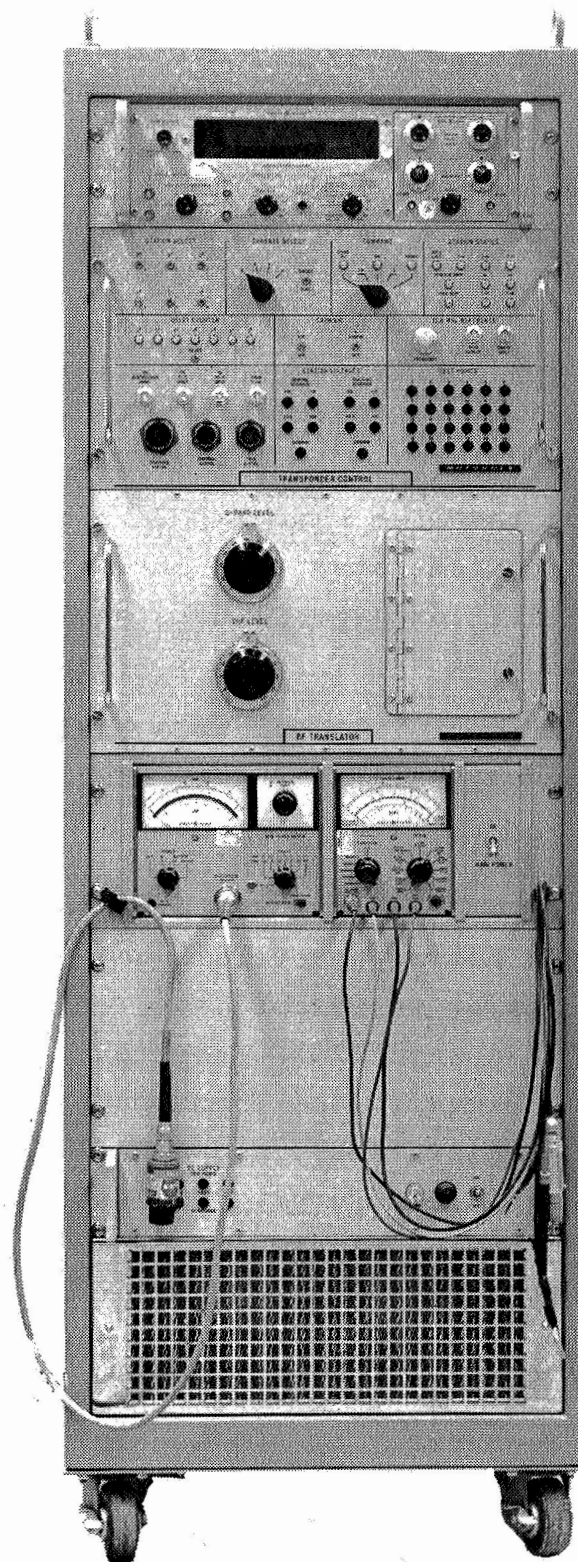
8.1 PURPOSE AND USE

The Transponder Checkout Equipment provides a test and calibration facility for the AROD transponder stations. It is intended to exercise the various operating modes of the transponder station and provide a visual indication of the current status of the station. Provision has been made to allow quantitative measurement of the more important operating parameters, such as threshold signal levels, acquisition times, and signal delay variations through the station.

The checkout equipment is a valuable tool for maintenance and troubleshooting of the transponder station.

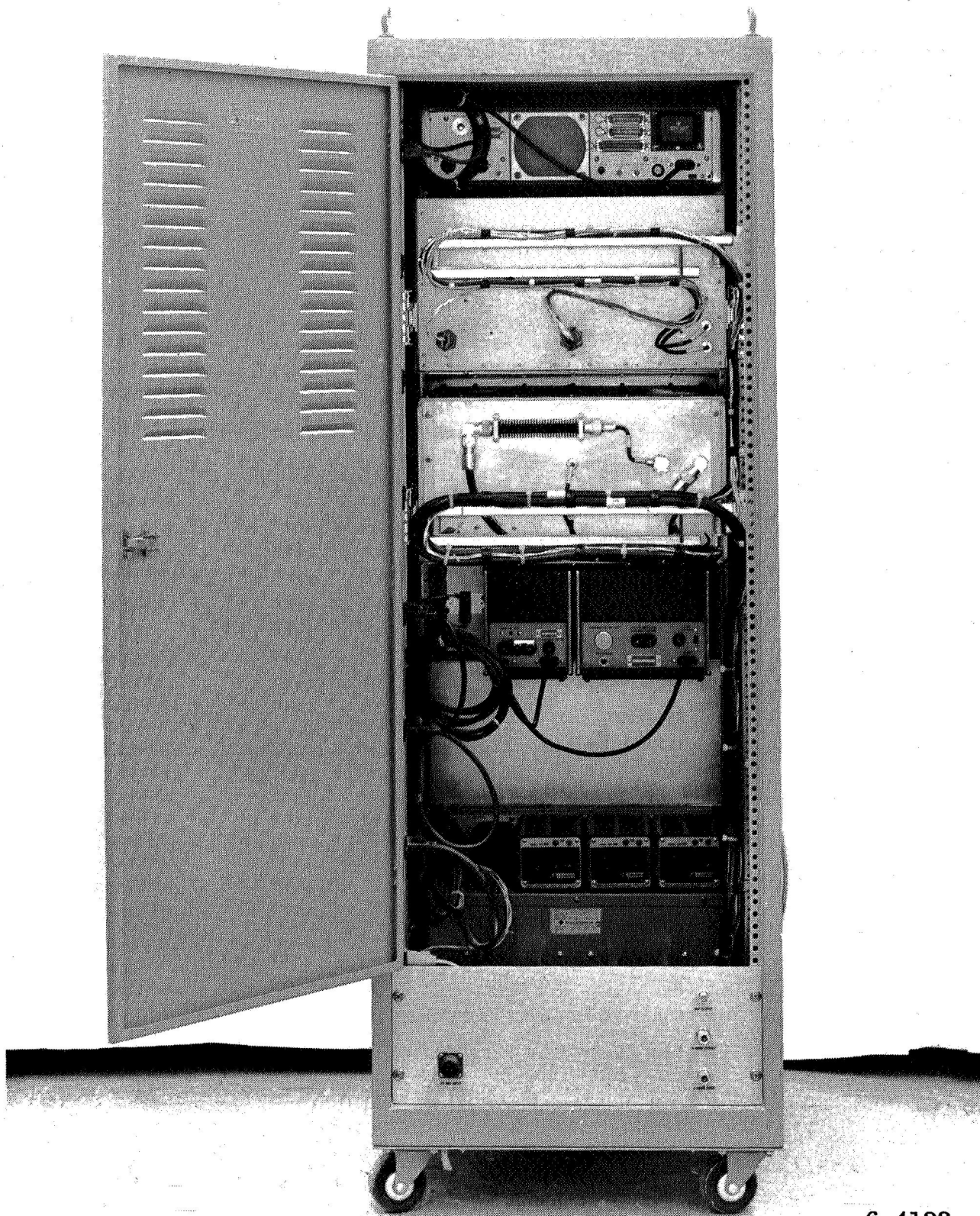
8.2 TEST SET DESCRIPTION

The main portions of the test set are housed in a standard 19-inch cabinet rack having an overall height of 5 feet. Referring to Figure 8-1, the major subassemblies, from the top of the rack down, are a Hewlett Packard 5245L Electronic Counter with a 5262A Time Interval plug-in, the Transponder Control Drawer (1A1), the R-F Translator Drawer (1A2), and a Hewlett Packard rack adapter frame containing an HP 431B Power Meter and an HP 410C Electronic Voltmeter. Mounted at the right-hand end of this frame is the Main Power ON-OFF switch, which controls the 115-vac power to a plug-in strip located in the rear of the rack. Next is an 8-inch blank panel below which are the Checkout Equipment Power Supplies (1A3), and a blower assembly to provide internal rack cooling. Auxiliary equipment, considered part of the Checkout Equipment, consists of a Tektronix 585A Oscilloscope and a Hewlett Packard 851A Spectrum Analyzer. These major assemblies are tabulated in Table 8-1. Figure 8-2 shows a rear view of the checkout equipment.



6-4121

Figure 8-1. AROD Transponder Checkout Equipment, Front View



6-4122

Figure 8-2. AROD Transponder Checkout Equipment, Rear View

TABLE 8-1. T-C/O Assemblies

| Assembly Name | Part or Model No. | Manufacturer | Reference Designation |
|--------------------------|-------------------|-----------------|-----------------------|
| Cabinet Assembly | 16-22619H01 | Motorola | 1 |
| Transponder Control | 01-22465H01 | Motorola | 1A1 |
| R-F Translator | 01-22466H01 | Motorola | 1A2 |
| Power Supplies, T-C/O | 01-28460H01 | Motorola | 1A3 |
| Frequency Counter | 5245L | Hewlett-Packard | - |
| Time Interval Unit | 5262A | Hewlett-Packard | - |
| Power Meter | 431B | Hewlett-Packard | - |
| Electronic Voltmeter | 410C | Hewlett-Packard | - |
| Blower Assembly | | | |
| Spectrum Analyzer | 851A/8551A | Hewlett-Packard | - |
| Oscilloscope | 585A | Tektronix | - |
| Oscilloscope Plug-In | 82 | Tektronix | - |

8.3 ASSEMBLY DESCRIPTION

All components within the rack assembly are panel-mounted with the exception of the 1A1 and 1A2 drawers, which are slide-mounted.

8.3.1 Transponder Control Drawer (1A1)

The Transponder Control Drawer (1A1) is shown in Figure 8-3. The major operating controls and status indicators, as well as interconnections to the transponder station, are located on the front panel. Located within the drawer are four R-F modules and six digital motherboards. The R-F modules are located on the left side of the drawer and the digital boards on the right. Figure 8-4 shows the location of these units. Reference designations have been assigned from 1A1A1 to 1A1A10 starting at the left rear R-F module and proceeding in a U-shaped pattern to

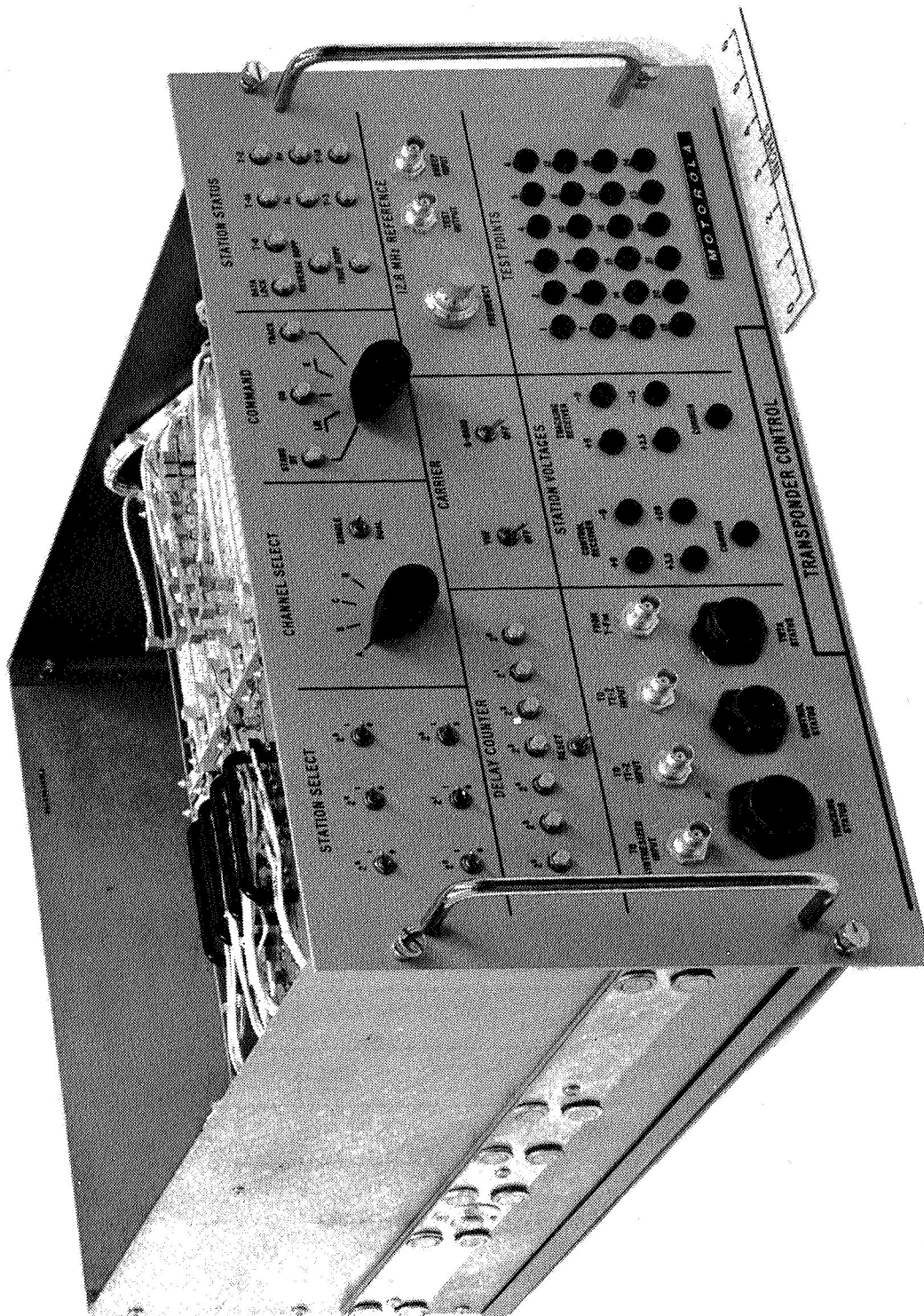
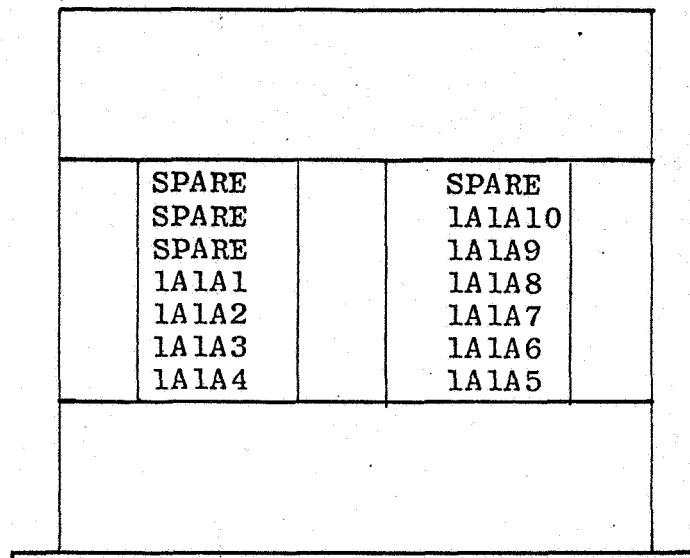


Figure 8-3. Transponder Control Drawer

6-4118



Top View
Module Location

| Reference Designation | Module Name | Part Number |
|-----------------------|-------------------------|-------------|
| 1A1A1 | VCO/Modulator | 01022670H01 |
| 1A1A2 | Synthesizer Multipliers | 01-22494H01 |
| 1A1A3 | Reference Generator | 01-22671H01 |
| 1A1A4 | Channel VCO's | 01-22672H01 |
| 1A1A5 | Lamp Drivers | 01-26375G01 |
| 1A1A6 | Delay Counter | 01-26372G01 |
| 1A1A7 | Synthesizer Dividers | 01-26366G01 |
| 1A1A8 | Code Generator | 01-26378G01 |
| 1A1A9 | Data Encoder | 01-26363G01 |
| 1A1A10 | Data Modulator | 01-26369G01 |

Figure 8-4. Transponder Control Drawer (1A1)

the right rear digital card. Connections to the R-F Translator (1A2) and Checkout Power Supplies (1A3) are made through the rear panel.

8.3.2 R-F Translator Drawer (1A2)

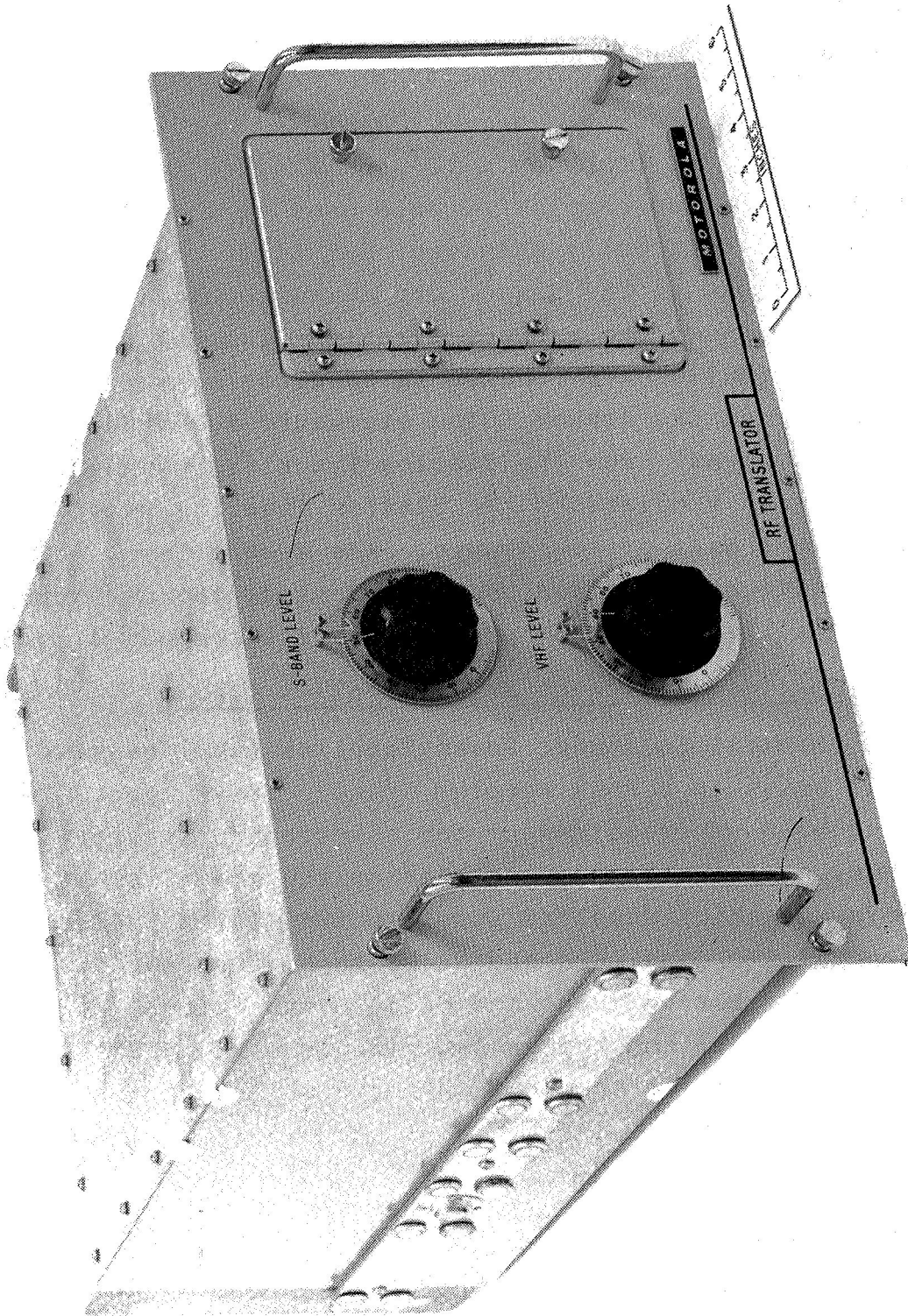
The R-F Translator Drawer (1A2) shown in Figure 8-5 contains the circuitry and components to generate and process the VHF, L-band, and S-band carrier signals used in the AROD Transponder Station. It is a fully shielded, R-F tight enclosure. The internal portions of the drawer are compartmentalized to provide isolation between the various signals. The VHF circuitry and D-C power distribution are located in separate compartments in the bottom half of the drawer. The circuitry required to translate the L-band signal from the Station Tracking Transmitter to the S-band signal required by the Station Tracking Receiver is located in the upper half of the drawer. The S-band level attenuator and output cable are shielded from the rest of the circuitry to prevent signal leakage when operating near threshold signal levels.

8.3.3 Checkout Equipment Power Supplies (1A3)

The Checkout Equipment Power Supplies (1A3) consist of three modular units in a rack adapter frame. These supply the ± 9 vdc and +3.5 vdc required by the electronic circuitry in the checkout equipment. Also mounted on the frame is a 6.3 vac transformer which supplies power to the status indicator lamps. An A-C line cord and an MS type connector on the rear of the unit provide input and output connections. An ON-OFF switch, a pilot lamp and an A-C line fuse are located on the front panel, as are test points for each of the three D-C output voltages.

8.3.4 Rack Cooling

Rack cooling is provided by a blower assembly at the bottom of the rack. Sufficient cooling is provided to maintain the internal temperature rise to 15°C or less.



6-4117

Figure 8-5. R-F Translator Drawer

8.3.5 Size and Weight

The sizes and weights of the subassemblies are given in Table 8-2.

TABLE 8-2. Equipment Sizes and Weights

| Subassembly | Dimensions, inches | | | Weight, lb |
|----------------------|--------------------|-------|-------|------------|
| | Height | Width | Depth | |
| Rack, complete | 60 | 21 | 28 | 375 |
| Transponder Control | 10-1/2 | 19 | 21 | 33 |
| R-F Translator | 10-1/2 | 19 | 22 | 42 |
| T-C/O Power Supplies | 5-1/4 | 19 | -- | -- |
| Power Meter Frame | 7 | 19 | -- | -- |
| Electronic Counter | 5-1/4 | 19 | -- | -- |
| Blower Assembly | 7 | 19 | -- | -- |

8.4 THEORY

8.4.1 Transponder Control Drawer 1A1

8.4.1.1 Functions

The Transponder Control Drawer is required to perform six major functions. These functions are:

1. Provide a 34.5-MHz signal which has had the station control data modulated onto it. This signal will be multiplied X4 in the Translator Drawer and form the 138-MHz carrier for the Station Control Receiver.
2. Provide any one of four signals which, after multiplication, will be the proper frequency to translate the Tracking Transmitter carrier to the Tracking Receiver carrier frequency.
3. Provide a reference signal to the Transponder Tracking Transmitter to make the L-Band Carrier coherent with the Checkout Equipment reference VCO during testing.

4. Provide a Z code sequence identical to the Vehicle Tracking Transmitter sequence. This will replace the normal Transponder Tracking Transmitter Modulation during testing so that, after translation to the proper carrier frequency, the signal appears to be coming from the vehicle.
5. Provide a means of accepting status information from the transponder and displaying sufficient information to keep personnel performing the tests informed as to the present state of the transponder.
6. Provide a means of measuring the differential delay through the S-band portions of the system.

8.4.1.2 Design Approach

The design approach used in the construction of the AROD Transponder Checkout equipment was to use, wherever possible, circuitry which had already been developed for either the AROD Vehicle or Transponder systems. The packaging concept chosen was that used in the AROD Transponder Station with the R-F circuitry housed in three-channel, plug-in modules and the digital circuitry on 6 x 6 plug-in motherboards. A simplified block diagram of the Transponder - C/O setup is given in Figure 8-6.

8.4.1.3 Theory of Operation

VHF Synthesizer

A simplified block diagram of the VHF synthesizer is shown in Figure 8-7. The output of the 34.5-MHz synthesizer VCO is mixed with the second harmonic, 25.6 MHz, of the reference VCO. This produces an 8.9-MHz signal which is within the operating frequency range of the programmable divider which follows. The output of the divider is fixed at 6.25 kHz to satisfy the system requirement that the VHF carrier can be spaced at 25-kHz increments anywhere within the 135 to 150-MHz band. To provide

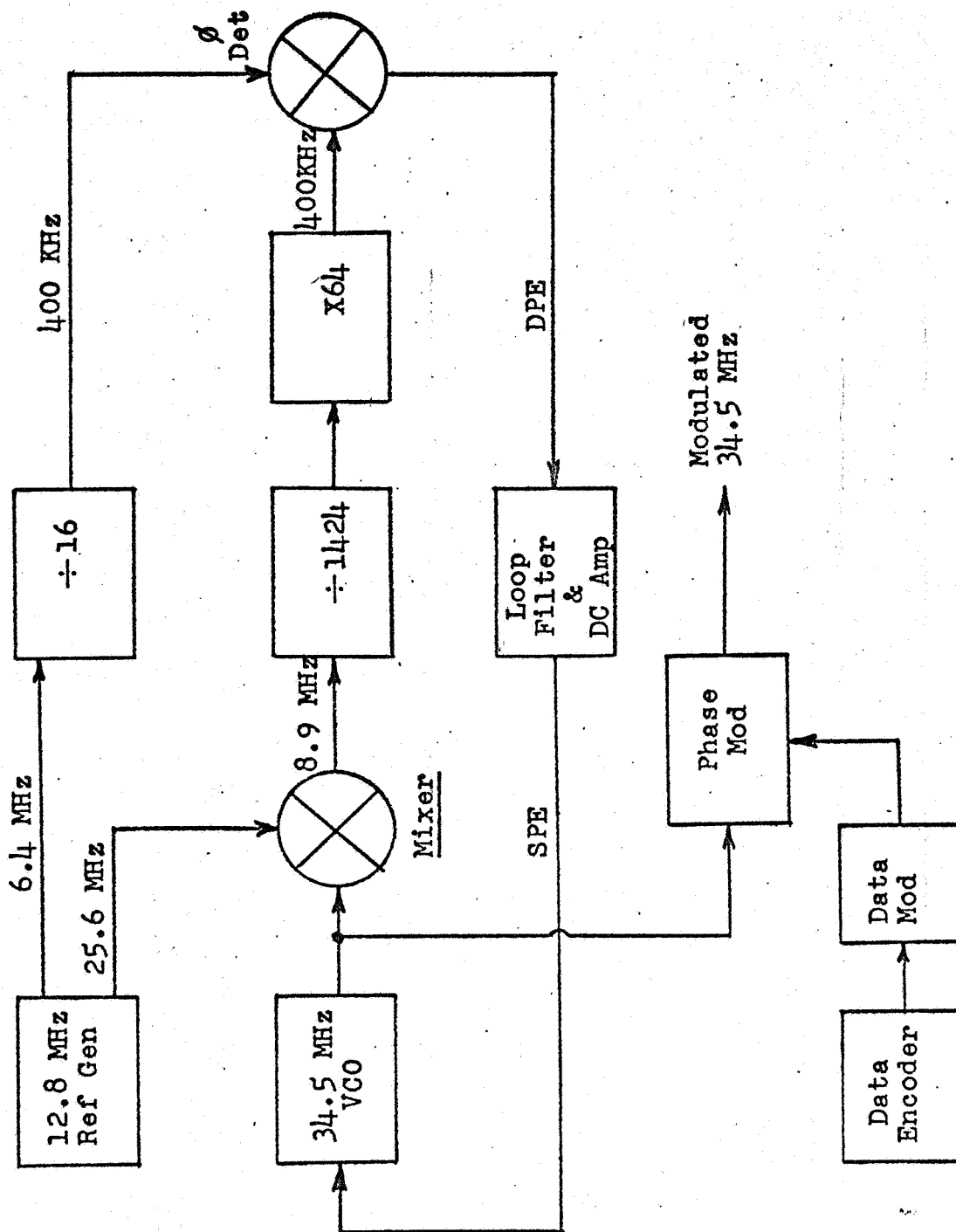


Figure 8-7. VHF Synthesizer - Block Diagram

additional loop gain, the divider output is multiplied to 400 kHz before phase comparison with a 400-kHz signal derived from the reference VCO. The phase detector is a digital "exclusive-or" circuit which produces an 800-kHz signal at its output. The phase error is represented by a variation in the symmetry of the square wave signal at this point. This signal is fed to the loop filter and D-C amplifier where it is filtered and amplified to provide the control voltage for the synthesizer oscillator. This closes the loop and phase locks the synthesizer VCO to the reference VCO. The loop is implemented as a second-order, Type 1 loop with a loop bandwidth, ω_L , of 100 Hz and a loop gain of about 6000.

Another output of the synthesizer VCO is fed to a phase modulator where it is modulated by an 18.75-kHz subcarrier which contains the station control data. The control data is generated in the data encoder. It is then used to phase shift key the subcarrier in the data modulator. The data modulator develops an 18.75-kHz reference signal and its two quadrature signals. The data gates these three signals such that a data ONE is represented by 18.75 kHz $\angle +90^\circ$ for the first half of the data bit interval and 18.75 $\angle 0^\circ$ for the second half. A data ZERO is represented by 18.75 kHz $\angle -90^\circ$ for the first half and 18.75 kHz $\angle 0^\circ$ for the second half.

Channel VCO's

A block diagram of the channel VCO loop is shown in Figure 8-8. One of the four oscillators is energized as determined by the channel select switch on the control drawer front panel. The same switch automatically sets the programmable divider to the proper ratio between 1033 and 1036 to keep the divider output constant at 6.25 kHz. The divider output is multiplied to 400 kHz before being phase compared to the 400-kHz signal derived from the reference VCO. This results in an increase in the loop gain by the multiplication factor. The phase detector output is fed to the loop filter and D-C amplifier where it is filtered and amplified to provide the control voltage for

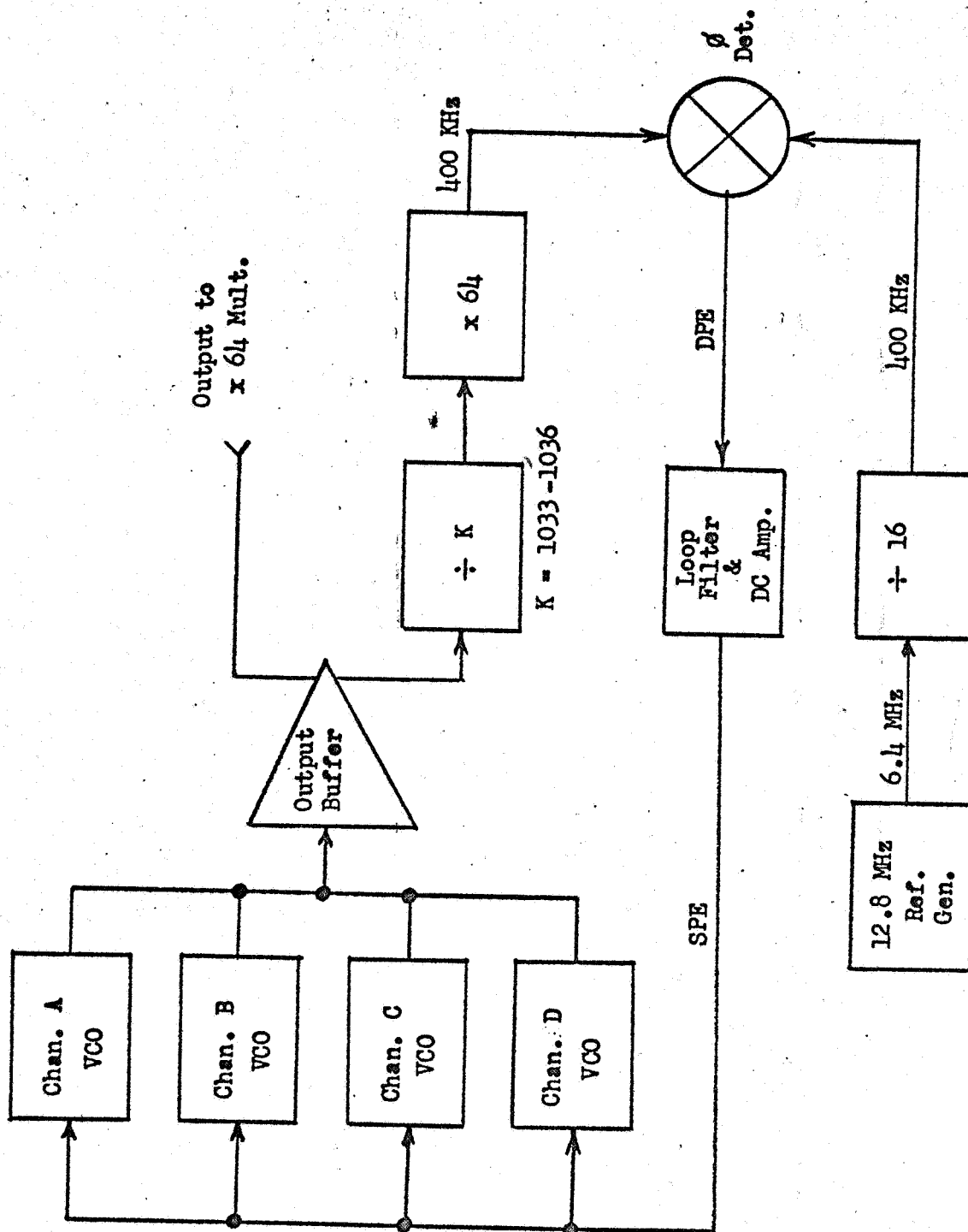


Figure 8-8. Channel VCO Loop Block Diagram

the channel VCO. This closes the loop and phase-locks the channel VCO to the reference VCO. The loop is implemented as a second-order, Type 1 loop with a loop bandwidth, B_L , of 10 Hz and a loop gain of about 4000.

The other output of the buffer amplifier is fed to the R-F Translator Drawer, 1A2, where it is multiplied X64 to produce the mixing signal required to translate the L-band signal from the Tracking Transmitter to the S-band carrier frequency of the Tracking Receiver.

Tracking Transmitter Reference

During normal operation, the 19.2-MHz reference signal for the Transponder Tracking Transmitter is supplied from the Doppler Inverter circuitry. This signal is replaced with a 19.2-MHz signal derived by multiplying the checkout equipment reference VCO X3/2 whenever the checkout equipment is being used. This results in the Tracking Transmitter output signal having a true Doppler offset no matter what the state of the Tracking Receiver. This is necessary in order to allow a simple translation of transmitter carrier to form the receiver carrier.

Code Generator

Since the Transponder Tracking Transmitter is, by translation, of the carrier frequency, used as a Vehicle Tracking Transmitter during testing, its normal range code modulation signal must be replaced by a signal corresponding to vehicle transmitter modulation. The proper combination of high and low code pseudo-noise sequences is generated in the Checkout Equipment Code Generator (1A1A8) and fed to the transponder where it is used to modulate the L-band carrier. The Code Generator is driven by the 12.8-MHz Reference VCO to assure coherence of all signals and the proper simulated Doppler shift for carriers and modulation.

Delay Counter

The Delay Counter, 1A1A6, is used to measure the time delay between the Checkout and Tracking Receiver range code clocks. The resolution is increased by a factor of 128 by first mixing the two 6.4-MHz clock signals, $T-F_{HS}$ and $C/O-F_{HS}$, with an internally generated 6.35-MHz signal. The resultant 50-kHz signals are fed to the set and reset input of a flip-flop. The flip-flop output is, thus, a pulse whose length is 128 times the delay between the two code clocks and will occur once for each time the reset switch on the front panel is depressed. This pulse is used to gate a 6.4-MHz square wave signal, $C/O-F_H$, into a seven-stage binary counter. The state of the counter stages is displayed visually on the front panel. The resolution of the counter is equivalent to $\frac{10^{-6}}{6.4 \times 128}$ or about 1.22 nanoseconds. The measurement is ambiguous for each full high code bit of delay. The number of full bits of delay may be determined by using an oscilloscope to compare the two codes. Each full bit of delay is equivalent to approximately 156 nanoseconds.

8.4.2 R-F Translator Drawer 1A2

8.4.2.1 Functions

The R-F Translator Drawer performs 2 major functions, which are:

1. Provide a means of multiplying the 34.5-MHz signal from the control drawer to the 138-MHz VHF carrier frequency and of controlling the signal level fed to the station control receiver.
2. Provide a means of translating the L-band carrier from the station tracking transmitter to the S-band tracking receiver carrier frequency and of controlling the level fed to the receiver.

8.4.2.2 Design Approach

The design approach used in construction of the R-F Translator was to use, wherever possible, commercially available components. Purchased components were used with the exception of the two R-F multiplier modules.

8.4.2.3 Theory of Operation

Reference to the R-F Translator Block Diagram, 69-20533J, will be very helpful during the following discussions.

VHF Circuitry

The 34.5-MHz signal from the control drawer is fed to the X4 multiplier module, 1A2A2. The 138-MHz signal out of the multiplier goes to a resistive power splitter. One of the splitter outputs is fed to the VHF monitor point located behind the R-F gasketed door on the front panel of the drawer. The other splitter output is fed to a 0-100 dB variable attenuator. The attenuator output can be adjusted from -50 dBm to -150 dBm and forms the VHF carrier signal to the station control receiver.

S-Band Circuitry

The L-band carrier from the station tracking transmitter is fed to a 30 dB, 15-watt attenuator located on the rear of the R-F Translator Drawer. (Provision has been made to easily bypass the attenuator when the TWTA is not being used.) The attenuator output is fed to a 10 dB directional coupler, with one output going to the L-band monitor point and the other to the S-Band Mixer. The reference signal for the mixer is formed by multiplying the channel VCO signal from the control drawer in the X64 multiplier module, 1A2A1. The two signals are summed by the mixer and a 2214-MHz bandpass filter is used to reject spurious signals at the mixer output. The signal is then fed through a PIN diode level set attenuator which provides about 10 dB of control on the signal level at this point. The signal is then split with one output going to the S-band monitor point and the

other to a 0-100 dB variable attenuator. The level set is nominally adjusted to allow the variable attenuator output to vary from -60 dBm to -160 dBm. This signal is fed to the Station Tracking Receiver.